Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

SHARC

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ANALOG DEVICES

Volume 28, Number 3, 1994

Editor's Notes

A BRIEF REPORT TO READERS

Two years ago, we started to ask specific feedback questions on the domestic "bingo" inquiry card. The first questionnaires were multiple-choice and rather lengthy; nevertheless a large percentage of you responded to the questions. More recently, the feedback questions have become simpler, unaided-recall types, at the bottom of the card: "Which articles did you like? Dislike? What would you like to see?" There were a heartening number of responses, including many suggestions. Most-of the readers of 28-1 who responded liked Oli Josefsson's first article on Σ-Δ converters and Walt Jung's article on voltage references. Early returns from 28-2 indicate that these two are again in high-scoring territory with Σ-Δ Part 2 and microphone preamps.

The "would like to see" responses were relatively flat across about 20 topical classifications, but audio, video, converters, DSP, motor control, tutorials, and "more!" rose somewhat above the surrounding terrain.

When we switched to self-mailers to save postage costs and get the environmental goodies from conserving plastic or paper envelopes, there was concern about the integrity of the "book" as received. So we added a question on the condition received. Only a few—1% of cards—reported "damaged, send replacement copy"; but that would still be several hundred if it were representative of the entire mailing. However, the damaged number has to be a lot less, because most recipients of damaged copies would return the card (which is well-protected at the centerfold) requesting a fresh copy. So the assumption is that those few cards represent most of the damaged copies. If we're wrong, and there are a couple of hundred of you out there gritting your teeth at the mangling of the *Dialogue*, please let us know! There were also about 5% in "fair" condition. If you don't like to have a "fair" copy, let us know and we'll replace yours, too.

GOOD LUCK, BILL

Bill Schweber, who has been a Senior Technical Marketing Engineer at Analog Devices and Contributing Editor to *Analog Dialogue* since 1987, has recently left us to join *EDN* magazine as Analog Editor, a job for which he is—alas!—eminently suited.

During this era, besides contributing counsel and articles to this publication, Bill has worked with engineers at all levels and locations within Analog Devices, with editors of trade publications, and with a wide range of technical people elsewhere in the world to develop interesting and useful stories about designs, technologies, and applications of Analog Devices products. His writing will not be totally new to *EDN* readers, since he has had a hand in many of their analog articles, whether authored by Analog Devices people or by *EDN* staffers.

In the course of his work, he has played a role in one of the most important aspects of professional development—encouraging, stimulating, and helping engineers to overcome their reticence to write technical articles (and to seek the rewards of authorship, especially professional visibility among their peers).

Bill's interest in writing has actually propelled his career development from systems engineer and design engineer to product manager, marketing engineer, and now, technical editor—with increasing visibility along the way. He has written numberless articles (for a current one, see page 3), and has authored three textbooks. The most recent is *Electronic Communication Systems—A complete course*, published by Prentice Hall (1991).

Bill has been fun to work with, an intellectually challenging colleague, an insatiable reader, an enthusiastic communicator, yet eminently practical, with a skepticism born of an intuitive feel for the downside (soft underbelly) of brilliant-sounding ideas (naturally, he is a "Dilbert" fan). We will miss him. Good luck, Bill!

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THE AUTHORS

Rupert Baines (page 8) provides marketing and marketing-communications support to Analog Devices's Communications Division. He has a BSEE from the University of Hull (United Kingdom) and an MBA from IESE in Barcelona (Spain), and has had experience in electronic design and international marketing communications. He has authored articles for the U.K. trade press on op amps, DSP, and RISC µPs.

Joe Buxton (pp. 13-16) , a Senior Product Marketing Engineer at Analog Devices, Santa Clara, has worked extensively on the development of SPICE op amp models. He writes application notes and articles for publication and is currently involved with business development and strategic marketing for linear products. In 1988, Joe received a BSEE from the University of California, Berkeley. In his leisure time, he enjoys bicycling, hiking, skiing, and listening to music.

(Biographies of **Steve Cox** (p.4) and **Doug Garde** (p.5) will appear in the next issue.

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Floating-Point DSP Leads in Memory, Interconnectivity, Performance

For single- and multiple processor applications, SHARC also provides upward compatibility.

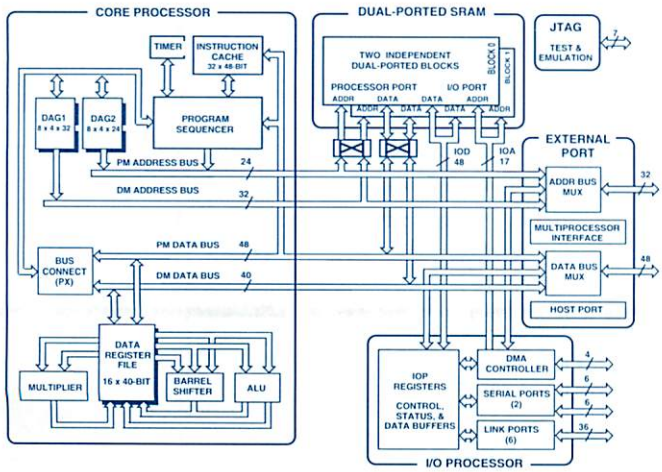
by Bill Schweber

The ADSP-21060 and ADSP-21062 are the industry's first DSPs in the class of **S**uper **H**arvard **AR**chitecture **C**omputer (SHARC™).* They integrate on a single chip: the industry's fastest general-purpose floating-point core, based on the ADSP-21020 (*Analog Dialogue* 25-2, 1991); a dual-ported 4- or 2-megabit SRAM; wide-bandwidth communication ports; and a sophisticated DMA (direct memory-access) controller—plus a crossbar switch to interconnect them (see block diagram below). Applications for SHARCs, in various configurations, are shown in the Table.

SHARC APPLICATIONS

	2-Mbit memory ADSP-21062	4-Mbit memory ADSP-21060
SINGLE PROCESSOR	•Low-cost color imaging (printers & scanners) •Low-end graphics (PC plug-in cards)	•Medical imaging
MULTI-PROCESSING	•Call processing •Digital cellular base stations •Data acquisition •Instrumentation	•Accelerator boards •Graphics boards •Image processing •Radar •Sonar

Featuring a processing speed of 40 MIPS (million instructions per second) and 120 MFLOPS (million floating-point operations per second), the ADSP-21060 SHARC combines the industry's highest-performance 32-bit floating-point DSP core—based on the ADSP-21020—with the largest on-chip memory of any processor—RISC, CISC, or DSP. Peripherals integrated on-chip



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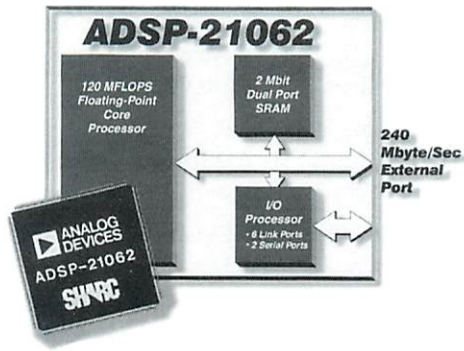

for high-speed I/O processing include: 10 simultaneous DMA channels; highly efficient host system/interconnect bus interfaces; external communication ports (6 link ports, 2 serial ports); and scalable multi-processing hooks. The ADSP-21060 and other processors in the SHARC family offer designers a single chip with clear advantages in performance, bandwidth, size and power over traditional DSPs and processors—and at a much lower system cost than designs based on standard DSP and embedded RISC-based chipsets.

Specific features of the ADSP-2060 SHARC include:

- 32-bit single-precision (or 40-bit extended precision) IEEE floating-point DSP core—with 3 independent, parallel computational units: ALU, multiplier, and shifter—featuring 40-MIPS performance, with 120 MFLOPS (millions of floating-point operations per second) peak, 80 MFLOPS sustained.
- On-chip, configurable memory banks—dual-ported 4-megabit internal SRAM—with fast, independent local memory access to DSP core, DMA controller, and I/O processor. The two banks support dual-operand fetch. (The ADSP-21062, with an identical processor, has 2 megabits of SRAM).
- I/O processor with DMA controller, memory mapper, and communications. Ten DMA channels, used with the dual-ported SRAM, handle background transfers between internal and external memory, peripherals, host, serial/link ports—without affecting performance of the DSP core. Two serial ports and 6 point-to-point links facilitate glueless multi-processor systems.
- Interface to off-chip memory, supporting programmable wait states and page-mode DRAM.

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- System bus crossbar, providing flexible interconnections between 16/32-bit host CPU, DMA device controller, external memory, peripherals, optional boot EPROM.
- On-chip hooks for "glueless" scalable parallel-bus cluster multiprocessing with up to six ADSP-2106x's for very high speed number crunching (see sidebar "Cluster multiprocessing").

The SHARC, like all Analog Devices DSPs, uses a "Harvard" architecture with two separately accessible address spaces (see *Analog Dialogue* 20-1 (1986) and 24-1 (1990). In its simplest configuration, one memory space is used for data, the other for program instructions. In contrast, the more familiar architecture used in conventional microprocessors (proposed by John von Neumann in 1948) uses a single stored program area, shared by both data and program. The hardware and interconnections for the von Neumann architecture are simpler, but its information bottleneck makes it less efficient at executing the highly repetitive algorithms of signal processing than the Harvard approach.

SHARC TOOLS

The tool set features the industry's first Numerical *C* implementation on a DSP processor. The ADSP-21000 Family G21K *C* Compiler supports Numerical *C* for vector and matrix operations, used extensively in DSP algorithms; this provides greater code efficiency and a more natural syntax for developing DSP applications, using fewer lines of code. Analog Devices' Numerical *C* has been adopted by the Free Software Foundation in version 2.4 of the standard GNU *C* Compiler.

The Simulator reflects all core changes of the ADSP-2106x processor, including the interrupt table, instruction set, register set and memory configuration. The Simulator also supports windowed access to DMA and SPORT (serial port) control and data registers, including simulated file I/O to serial ports. In addition, the Simulator supports DMA operation to/from an external device and DMA operation to/from external memory. External devices are supported using file I/O. Memory access may be tracked in two ways: either by a "memory window", displaying a specified range of memory, or by tracking the "data fetch" address. In addition, the ADSP-2106x Simulator and EZ-ICE Emulator both feature a graphical user interface with the same intuitive menu layout. All are integrated with the CBUG™ *C* Source-Level Debugger.

The ADSP-2106x EZ-ICE™ In-Circuit Emulator, with its easy-to-use Microsoft Windows® interface, allows non-intrusive access to the internal processor registers through a JTAG serial boundary-scan interface. Consisting of a PC plug-in card and a small attached probe, it supports full-speed operation, multiprocessor debugging, up to 30 software breakpoints, nine hardware break ranges, single-step execution, register Modify and Read, and program- and data memory upload/download.

The ADSP-21062 EZ-LAB is a PC plug-in development system that includes an ADSP-21062, with connectors for at least four more. It has a connector for analog front end cards and includes an AD1847 sound-codec card. Software is included for program debugging. The ADSP2106x-EZ-KIT package includes the EZ-LAB plus development software (assembler, linker, simulator, PROM splitter, *C* compiler with Numerical *C* support, *C* source-level debugger, and *C* runtime library). EZ-LAB is priced at $1,495 and EZ-KIT at $1,995.

Both SHARCs are housed in 240-lead PQFP packages with enhanced thermal conduction. The 2-megabit ADSP-21062 for 5-V supply is sampling now, with full production by March 1995; the 4-megabit ADSP-21060 will be sampling in March 1995 and in full production by June. They are priced at $296 for the ADSP-21060 and $196 for the ADSP-21062 (1000s).

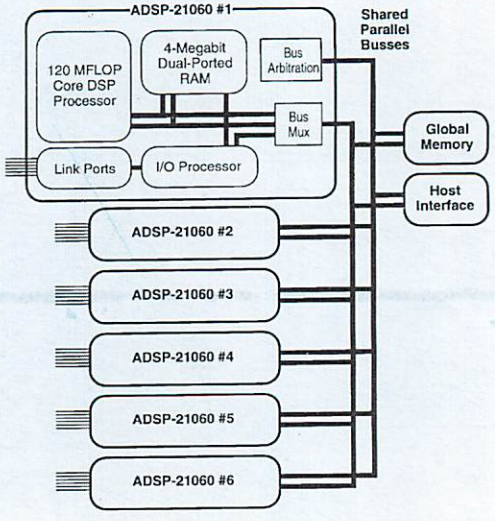
CLUSTER MULTIPROCESSING
DSP Communication through Shared On-Chip Memory

by Steve Cox

Multiprocessor systems typically use two schemes to communicate between processor nodes. One approach uses dedicated point-to-point communication channels. In the other, nodes communicate through a single shared global memory via a parallel bus. The ADSP-2106x SHARC supports both, implementing point-to-point communication through its six Link Ports, and realizing an enhanced version of shared parallel bus communication called *cluster multiprocessing*.

Cluster multiprocessing is embodied with up to six nodes on a parallel bus that allows internode access to on-chip memory, to a shared global memory, and to a host processor interface. The cluster configuration allows the ADSP-2106x to have a very fast node-to-node data-transfer rate. It also allows for a simple, efficient communication model. For instance, all the required setup for a DMA transfer can be done by a node on one side of the data transfer. The other node is not interrupted until the data transfer is complete. Each processor can directly read from and write to another processor's internal memory. This distributed-memory multiprocessing system also simplifies the software communication model.

The figure shows a cluster of such DSPs. Up to six processors and a host can vie for the bus without any additional external logic. Bus requests are made implicitly whenever a processor accesses external address space. Because each processor monitors all bus requests and applies the same priority logic to the requests, each can independently determine who will be the next bus master. The on-chip arbitration logic allows transitions in bus ownership to use only one cycle of overhead. Once a processor gains ownership of the bus, it has access not only to external memory but also to all the other processors' internal memory and I/O registers. Thus, a processor can directly transfer data with another processor or set up a DMA channel to transfer the data. Memory-to-memory transfers can occur at a 40-MHz, 240-megabyte-per-second rate.



To identify the address space of each processor within the unified address space of the cluster, each processor has its own unique ID. The I/O registers, internal memory and external memory are all part of the unified address space.

The DSP's internal memory is designed to complement the I/O needs of multiprocessor systems. The on-chip dual-ported RAM allows full-speed interprocessor transfers; at the same time, it supports dual accesses by the floating-point DSP core. No extra cycles are ever required from the DSP core; thus the processor's full 40-MIPS, 120-MFLOPS performance is easily achieved.

A bottleneck may exist within a cluster, because only two nodes can communicate on the shared bus each cycle. Other nodes are held off until the bus is released. Since the ADSP-2106x also supports Link Port communication within a cluster, this bottleneck can be eliminated, because all 6 ports can communicate simultaneously. However, individual transfers occur at 40 Mbyte/s; a lower rate than that allowed on the parallel bus. Since the Link Port data path is narrower than the node's native word size, the transfer of each word requires multiple clock cycles. Link Ports may also require more software overhead and complexity because they must be set up on both sides of the channel before they are used.

ON-CHIP SRAM DESIGN CONSIDERATIONS

Designer challenges and user opportunities in a DSP with on-chip mega-memory

By Doug Garde

Integration of a processor with substantial amounts of memory allows a chip designer to use SRAM in new and creative ways. No longer is the memory a non-optimal fixed function over which the designer has no control; instead, one can take advantage of many synergies that exist in defining its operation and interfacing it with the processor. To understand these differences, we need to review some issues associated with interfacing to external SRAM.

Considerations for interfacing to external SRAM: In high speed systems (i.e., 25-ns cycle time or less), the most significant challenge in accessing external memory is meeting the time budgets. In each cycle, the processor must drive the address off-chip, and then wait for the external memory to access the data and drive it back to the processor. In addition, the processor must provide accurately timed read and write strobes to the memory. Furthermore, the data and address buses typically have 50 to 100 pF of capacitive loading, which adds to the bus charging time.

Unless wait states are used, expensive, fast-access memories are needed. In a 25-ns cycle for instance, the external memory might typically require a 10-ns read-access time (17 ns in SHARC). These requirements make the SRAM very expensive and power-consuming.

In addition, because of the fast transition times required on each signal, ringing and large ground and power supply transients occur, producing a large amount of noise that reduces signal integrity. Considerable design skill and expensive printed circuit boards are needed to overcome these noise problems. Power dissipation also increases, due to the large number of address and data lines being charged and discharged. Package pin-count usually increases, because two sets of buses (for two external memories) are needed per cycle in Harvard and Super-Harvard architectures.

The principal benefits of off-chip memory are that memory size can be customized to the application, and the processor chip—without memory real-estate—is smaller and cheaper.

Considerations for the Design of Internal memory: The designer of an on-chip memory can customize both the memory and the interface to achieve performance and functionality that could not be attained with external off-the-shelf memory. First, the interface between the processor and memory can be simplified because both are run by the same clock. Synchronous, or *clocked*, memory can operate faster than asynchronous or unclocked memory, but most commercial SRAMs are asynchronous because of the way they have evolved in the commercial marketplace. Since they are standardized, their prices are lower than for speciality SRAMs.

With the address and data buses internal, far less time is wasted driving large off-chip drivers and external buses; this allows more of the time budget to be available for the memory access. Performance is further improved by the use of address and data latches at the memory and of clocked sense amplifiers (no address-transition detection circuits are needed). Since both memory and processor are part of the same silicon, the process and temperature variations track, eliminating the need for excessive best-case/worst-case tolerances.

In fact, the memory access requirements are eased so much that *two accesses per cycle* are possible on-chip, whereas even one access is a challenge for off-chip memory. Dual internal accesses per cycle are used in the ADSP-21060 SHARC family. This produces improved processor performance, or alternatively allows an I/O operation, such as DMA, that is independent of the processor access.

On-chip memory also makes it easier for many buses to be multiplexed for flexible access to multiple memory blocks. For example, each of two memory blocks could be easily accessed by either the program sequencer, either one of two address generators, or an I/O processor. This flexibility means that only one external memory is needed to supply data or programs, and therefore only one set of external buses is needed. Data and programs can be transferred as a background operation using an internal DMA controller. Furthermore, because this is usually not time-critical, the external memory, can often be inexpensive page-mode DRAM with wait states.

Yet another benefit of on-chip memory is the ease of designing a memory that allows access to either larger or smaller memory words in a single block. For example, on the ADSP-21060 SHARC, a normal data word is 32 bits, a short word is 16 bits and a long word for instruction or extended precision is 48 bits. All these word types can be intermixed in a single block of on-chip memory by designing columns to be 16 bits wide. By decoding the column addresses in groups of 1, 2 or 3 columns, corresponding to 16, 32 and 48 bits, the memory space can include each data type while still providing full memory utilization. This allows the use of internal memory to be customized to fit the application.

Fast, Low-Distortion V-Feedback Op Amps Offer Optional Accurate Clamping

With 175/180-MHz large-signal BW, AD9631/9632 have ultralow distortion; AD8036/8037 have voltage-variable clamped output

The AD9631, AD9632, AD8036, and AD8037* voltage-feedback op amps, manufactured on the Analog Devices XFCB (eXtra-Fast Complementary Bipolar) process, provide outstanding performance at low cost. The **AD9631** & **AD8036** are unity-gain stable (G ≥ +1); and the **AD9632** & **AD8037** excel for applications with voltage gain magnitudes ≥ +2 V/V or –1 V/V. Performance of both families is fairly similar, except that the **AD8036** & **AD8037** have an additional pair of voltage inputs, V_H and V_L, that provide simple, fast, flat, accurate clamps on the output for input voltages $\geq V_H$ or $\leq V_L$, when operated in the noninverting connection.

When connected for gain of +1, the AD9631 has small-signal bandwidth (–3-dB) of 320 MHz (220 minimum) and large-signal (4 V p-p) BW of 175 MHz (150 min). Corresponding BWs for the AD9632, with a gain of +2, are 250 (180) MHz and 180 (155) MHz. All of these devices typically have flat response (<0.1 dB) to 130 MHz (Figure 1). Performance characteristics for all four types are compared in the table. They are available for the –40 to +85°C temperature range, housed in SOIC and miniDIP packages. Prices start at $4.12 in 1000s.

Typical (min/max) performance characteristics

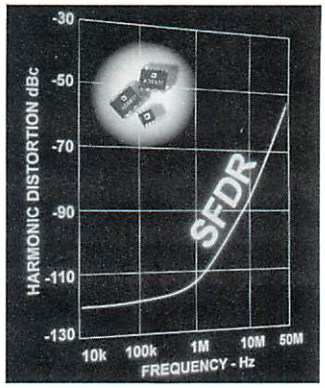
[$\pm V_S$=±5 V, R_L=100 Ω, unless noted otherwise]

	AD9631 [G=+1]	AD9632 [G=+2]	AD8036 [G=+1]	AD8037 [G=+2]
Bandwidth, MHz, small signal	320(220)	250(180)	240(150)	270(200)
Large signal, [unclamped]	175(150)	180(155)	195(160)	190(160)
0.1-dB flatness	130	130	130	130
Slew rate,V/µs,average ±, 4-V step	1300(1000)	1500(1200)	1200(900)	1500(1100)
Settling time to 0.1%, ns, 2-V step	11	11	10	10
Distortion, dBc, 2nd har. R_L=500Ω	–72(–65)	–72(–65)	–66(–59)	–72(–65)
Voltage noise, nV/√Hz, 1-200MHz	7	4.3	6.7	4.5
Differential gain error,%, 3.58 MHz	0.03(0.06)	0.02(0.04)	0.05(0.09)	0.02(0.04)
Differential phase error, °,3.58 MHz	0.02(0.04)	0.02(0.04)	0.02(0.04)	0.02(0.04)
Phase nonlinearity,°,DC-100 MHz	1.1	1.1	1.1	1.1
Voltage drift, µV/°C, –40 to +85°C	±10	±10	±10	±10
Bias current, µA, –40 to +85°C	2(7)	2(7)	4(10)	2(7)
Output voltage range, V, R_L=150Ω	±3.9(3.2)	±3.9(3.2)	±3.9(3.2)	±3.9(3.2)
Output current, mA	70	70	70	70
Supply voltage range, V	±3-±6	±3-±6	±3-±6	±3-±6
Quiescent supply current, mA	17(18)	16(17)	20.5(21.5)	18.5(19.5)
Clamp voltage range, V [V_H or V_L]			±3.9(3.3)	±3.9(3.3)
Clamp accuracy, mV (2× overdrive)			±3(5)	±3(5)
Clamp input bandwidth, MHz [–3 dB]			240(100)	240(100)

As Figure 2 shows, response is exceptionally clean, with SFDR† well below –110 dBc at frequencies up to 1 MHz, increasing to only –95 dBc at 5 MHz, and a maximum of –65 dB 2nd harmonic

†Spurious-Free Dynamic Range, the dB difference between the rms amplitude of a single-tone signal and the largest spurious peak (usually the 2nd harmonic) within the bandwidth of interest.

*Use the reply card for technical data. Circle 2



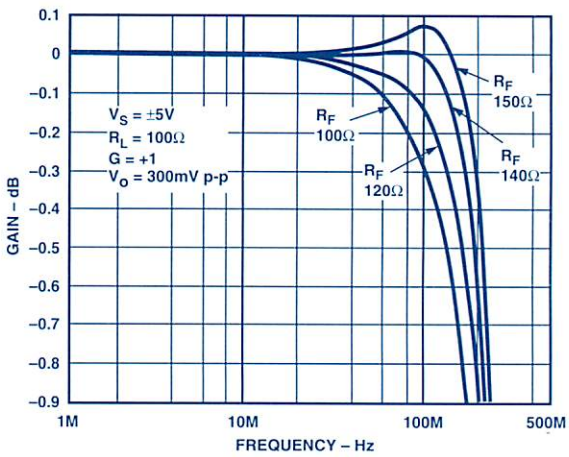


Figure 1. AD9631AN small-signal 0.1-dB flatness. (For AD9631AR, add 20 Ω to R_F)

at 20 MHz (AD9631 with 500-Ω load). Distortion figures are comparable for the AD9632, taking into account the doubled gain: 2nd harmonic distortion is only –95 dB at 1 MHz and a guaranteed maximum of –65 dBc at 20 MHz. The AD8036 and AD8037 have similar performance, –100 and –95 dBc typical at 1 MHz, and –59/–65 dBc guaranteed for AD8036/37 at 20 MHz.

With their voltage-feedback architecture, these wideband, low-distortion, fast-settling operational amplifiers meet the requirements of many applications which were typically in the province of current-feedback types. They bring the improved predictability of a classical op-amp architecture to buffer circuits for A/D converters, video line drivers, and active filters. Many types of filter circuits benefit by the flexibility obtainable with the balanced high-impedance input circuits of these amplifiers.

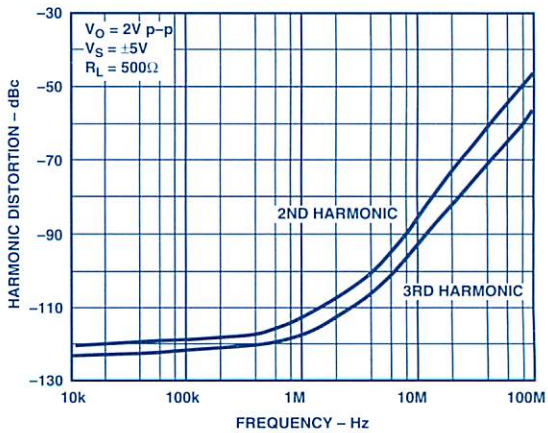


Figure 2. AD9631 harmonic distortion vs. frequency, G = +1 V/V, R_L = 500 Ω.

Figure 3 shows a circuit for applying the AD9631/AD9632 as a line driver for a back-terminated 75-Ω video cable. Many details that must be considered in the use of op amps in designing line drivers in general, and video line drivers in particular, can be found in *Analog Dialogue* 26-2, "Op amps in line-driver and receiver circuits", by Walt Jung.

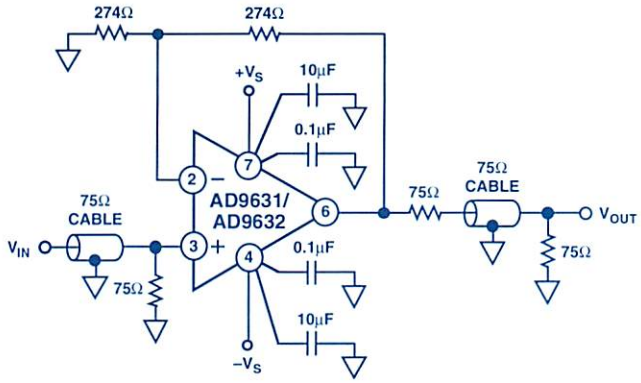


Figure 3. AD9631/AD9632 as video line driver.

ABOUT CLAMP AMPLIFIERS

A clamp amplifier is a limiting or bounding circuit. For input voltages between two levels, V_H and V_L, the output is proportional to the input. For inputs greater than V_H or less than V_L, the output ideally remains constant, bounded at V_{CH} or V_{CL} (V_H or $V_L \times$ the amplifier gain, A_V), irrespective of the input, as shown in Figure 4a. The threshold voltages, V_H and V_L, may be fixed or variable. If the amplifier can handle positive and negative input/output voltages, V_H and V_L can have any plus or minus values within the specified range, as long as $V_H > V_L$.

Clamp amplifiers may clamp the output voltage (OCL) or the input voltage (ICL). The AD8036/37 use CLAMPIN®, a highly precise ICL design: comparators quickly and accurately steer to the actual plus input of the amplifier the lesser of V_{IN} and V_H, and the greater of V_{IN} and V_L. The amplifier gain amplifies V^+.

When controlled by external voltages, a clamp amplifier circuit is characterized by linearity (low distortion) in the unclamped range, flatness in the clamped range, accuracy of setting of the clamp voltages, and sharpness of the transition. Dynamically, when driven rapidly (i.e., stepped) into the clamped zone, it must have low overshoot and quick recovery. If V_H and V_L are variable control voltages, bandwidth must be adequate to handle them.

The AD8036 and AD8037 perform the clamp function with better performance than any available IC alternatives. Specifications include a clamp-voltage range of ±3.9 V (3.3 V min), clamp accuracy/flatness to within ±3 mV (5 mV max), a "knee" region of 100 mV. Maximum overshoot is 5% max in response to a 2× step overdrive, with recovery within 1.5 ns. The clamp input responds with a –3-dB bandwidth of 240 MHz, a useful feature when the clamp inputs are used to modulate an r-f signal.

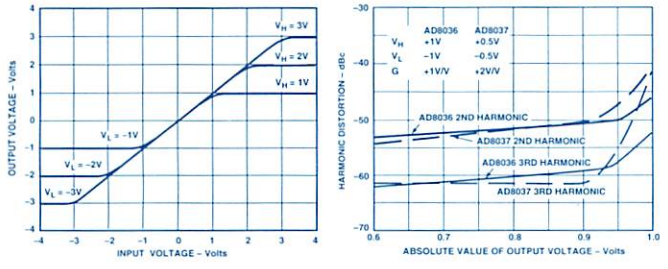


Figure 4. (a) Clamp amplifier performance, for representative clamp values, V_H and V_L, showing flatness and small "knee" area. (b) Harmonic distortion as output amplitude approaches clamp voltage. V_o = 2 Vp-p, R_L = 100 Ω, f = 20 MHz

To demonstrate how "clean" the clipping is, Figure 4b plots 2nd- and 3rd-harmonic distortion as a function of sine-wave amplitude as it approaches a ±1-V output clamp setting. The approach to the clamped region contributes no additional distortion for a >90% swing; and even *at the clamp threshold*, the worst distortion seen is only 1% (–40 dB).

Applications: Figure 5 shows a basic circuit for clamping with gain; here, the gain is 2 V/V, and the resulting output clamp levels are 2 V_H and 2 V_L. In this configuration, with the 0.1-μF bypass capacitors, V_H and V_L are assumed to be fixed or slowly varying. The clamp-level signal sources must be able to supply dc bias currents of 70 μA max without error.

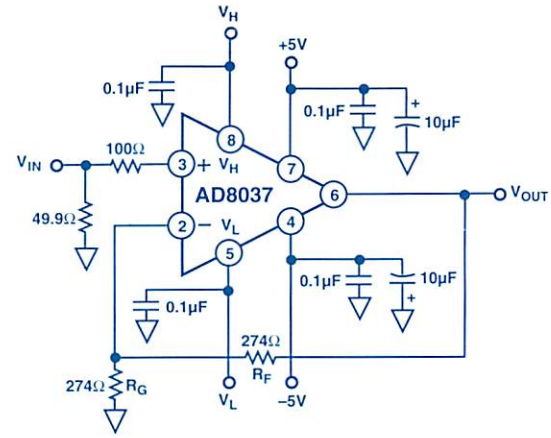


Figure 5. Basic clamp amplifier circuit for gain of +2 V/V.

Clamp amplifiers are useful as protective buffers for A/D inputs, as programmable flat-pulse-forming amplifiers, and as amplitude modulators. Because V_H and V_L clip in the input stage and have input bandwidths comparable to the signal inputs, they can also be used in simple circuitry to generate the positive or negative absolute value of input signals (i.e., full-wave rectify them). Figure 6 shows a TTL-based programmable pulse generator.

These amplifiers were designed by Roy Gosser at our facility in Greensboro, NC.

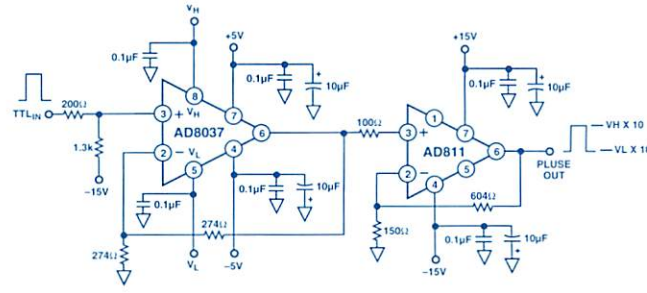


Figure 6. Programmable flat- pulse generator application with TTL input and up to 24 V p-p output with 2500-V/μs slew rate.

New High-Speed A/D Converters for Communications

12-Bit AD9022/23/26/27 offer sampling at up to 31 MSPS with SFDRs up to 76 dB

by Rupert Baines

Four new 12-bit analog-to-digital converters, the TTL-compatible AD9022 and AD9026 and the ECL-compatible AD9023 and AD9027, combine high sampling rates (as high as 31 MSPS) with extremely low distortion (SFDR as high as 80 dB). They are intended for applications in wideband communications systems or instrumentation where high-frequency signals must be accurately captured and digitized.

Typical applications for these devices include systems for detecting high-frequency signals in the midst of a welter of other signals. Analog input-bandwidths as high as 200 MHz (extending well beyond Nyquist) mean that signals can be captured using undersampling. Instead of a local oscillator and mixer, the converter's sample rate is used to alias a signal down to baseband. If such an application is truly to detect weak signals, a wide dynamic range is required; this implies high resolution with low distortion and noise.

The **AD9026** and **AD9027*** are optimized for communications applications, while the **AD9022*** and **AD9023*** are intended for applications where low distortion at low cost is more important than getting the very highest speed. With sampling rates of 20 MSPS they can capture a 9.6-MHz bandwidth with SFDRs of 74 and 72 dB.

The 31-MSPS specifications of the AD9026B and AD9027B are significant because the US cellular communications industry (both analog and the TDMA digital standard) uses a 30-kHz channel; a 31-MSPS sampling rate allows 1024× oversampling (30.72 MSPS = 10-24 × 30 kHz). A traditional cellular system has a narrowband receiver for each channel—up to 60 receivers in a typical base station. In contrast, it is possible to use a wideband receiver based on the AD9027 to digitize the entire cellular bandwidth (12.5 MHz), with resolution high enough for DSP techniques to be be used to extract any of the desired channels digitally. A single wideband receiver can thus replace as many as 60 narrowband front ends (see Figure 1). Because the tuning is done in software (by the DSP), it is possible to change between standards (e.g., from AMPS to TDMA) merely by loading a new program.

With the ability to digitize a 15-MHz portion of the spectrum directly, the AD9026/27 make possible a range of new communications products in which RF and IF signals will be handled digitally in much the same way that audio and video signals are today. Besides cellular infrastructure, the first applications are likely to be advanced instrumentation, such as spectrum analyzers, ultrasonic imaging devices and communications test-sets.

INTERNAL STRUCTURE

The devices use a three-pass subranging architecture (Figure 2). Two track-and-hold amplifiers (T/H), three flash ADCs, two DACs and two residue amplifiers produce a 14-bit digital word that, digitally error-corrected, results in a 12-bit-accurate output. The input T/H amplifier is the most critical block, because it must sample a ±1.024-V signal to better than 12-bit accuracy; errors introduced at this stage can't be corrected later.

Unlike many wideband ADCs, the dc performance of these devices needs no apology. No-missing-code operation is guaranteed, while differential & integral non-linearity are a maximum of 1 and 3 bits, respectively. All three specifications are guaranteed over

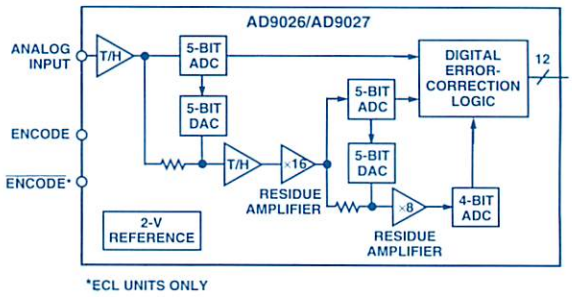


Figure 2. Block diagram of 3-pass subranging architecture.

the entire operating temperature range of –25°C to +85°C (case temperature). The specified power-supply is +5.0 V, –5.2 V, and dissipations are 1.4-1.6 W. All four types are available in 28-pin ceramic DIPs; and the AD9022 and AD9023 are also available for surface mount. Prices (1000s) start at $140 for the AD9022/23 and $238 for the AD9027/28.

These converters were designed by Frank Murden and Dana Zipperer, of ADI's Communications Division, in Greensboro, NC.

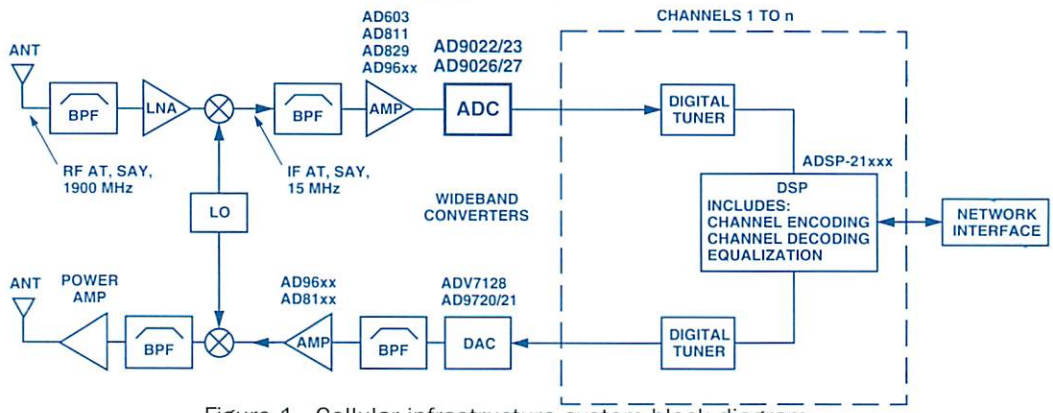


Figure 1. Cellular infrastructure system block diagram.

*Use the reply card for technical data. Circle 3

New 8-Bit, 16-Channel Voltage-Output D/A Converters

AD8600 has 16 multiplying DACs with double buffering and readback, ±1-LSB total unadjusted error, and 2-μs settling time

The AD8600* combines 16 high-performance multiplying, 8-bit D/A converters in a single monolithic IC. A parallel-input device, with double buffering, it can accept data clocked in at speeds up to 12.5 MHz, a combination of speed and high channel-count unmatched in the industry. It is specified to operate on a single +5-volt supply or dual ±5-V supplies, has a total unadjusted error within ±1 LSB, settles to within ±1 LSB of final value within 2 μs of reference voltage changes or data updates, and consumes only 175 mW max in single-supply applications.

With its ability to furnish up to 16 independent voltages simultaneously, it is useful in multichannel instrumentation and test systems requiring speed and 8-bit accuracy. Typical applications include multichannel instrumentation systems, automatic test equipment, phased-array ultrasound gain adjustment, setting threshold levels for 16-channel logic analyzers, and PC-compatible programmable data-acquisition and control cards.

Figure 1 shows the device's functional organization and connections. An 8-bit parallel data input, four address pins, and $\overline{CS}$, $\overline{LD}$, $\overline{EN}$, R/$\overline{W}$, and $\overline{RS}$ provide the digital interface. The DACs all share a common external reference voltage, which sets the full-scale output. The device is housed in a 44-lead PLCC and is specified for operation from –40 to +85°C. The AD8600AP is priced at $25.28 in 1000s.

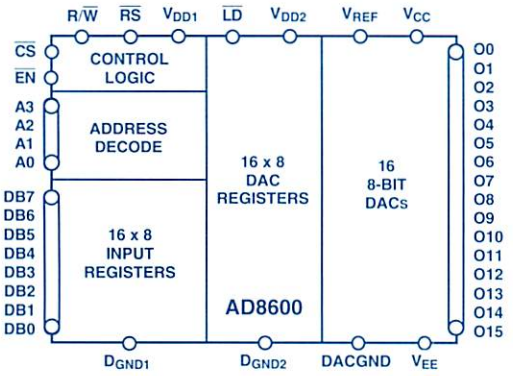


Figure 1. Functional block diagram.

The signal flow in each DAC channel, including readback, is shown in Figure 2. Data appearing on the 8-bit parallel bus is clocked into each input register, then all DAC registers are updated simultaneously, producing buffered output voltages that can range from 0 to (V_{CC} – 1 V). At system power-up, or during fault recovery, the reset ($\overline{RS}$) pin forces all DAC registers into the zero state, which places 0 V at all DAC outputs.

*Use the reply card for technical data. **Circle 4**

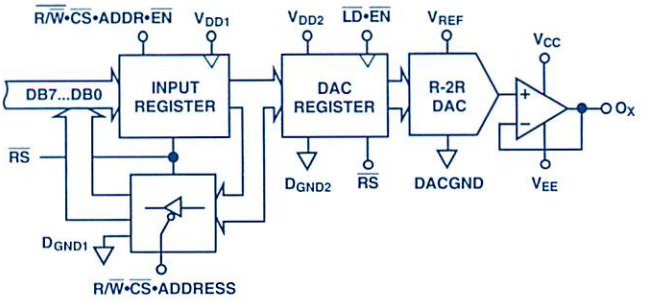


Figure 2. Equivalent DAC channel, showing double-buffering of the digital inputs, digital readback, and output voltage buffering.

Application: Time-dependent variable-gain amplifier. The AD8600 is useful in phased arrays for ultrasound imaging as a gain-control signal for an exponential amplifier, such as the AD600 X-AMP® (*Analog Dialogue* 26-2, 1992). X-AMPs are variable-gain amplifiers for which equal increments of control voltage increase the signal gain in equal dB steps. For example, the control voltage increment corresponding to a 6-dB step increase results in a doubling of voltage gain.

In medical ultrasound, bursts of ultrasound are applied to the subject, then a set of transducers picks up the reflected sounds at various locations. The timing and strength of echoes from structures within the subject produce a picture of the internal situation.

However, because the ultrasound energy is absorbed as well as reflected, the deeper the source of the echo, the smaller the signal that is returned. To resolve far objects accurately, the gain on the returned signal must be greater than for near objects. Since the propagation speed and absorptivity of the medium are knowable, the rate of exponential attenuation can be predicted. This information can be used correspondingly to increase the gain of an X-AMP associated with a given transducer so as to make possible accurate estimates of the strength of the reflected signal, irrespective of depth.

D/A converters can be used to apply the required programmed control voltages to the X-AMP associated with each transducer. The AD8600 is especially useful in this application because it can be used compactly and at low cost to control the gains of an array of transducer channels with the required speed and accuracy. Figure 3 shows a scheme of digital exponential gain adjustment applied to one channel of an array.

The AD8600 was designed by Derek Bowers and Carol Flores at our Santa Clara, CA facility.

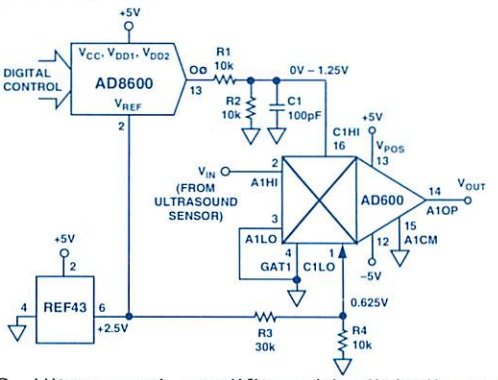


Figure 3. Ultrasound amplifier with digitally controlled variable gain.

Low-Cost 16-Bit DAC for Communications, Imaging, & Displays Updates at 30 MHz

Current-output AD768 has on-chip reference, low quantization noise, 14-bit linearity, 83-dBc SFDR

The AD768*, a wideband high-resolution D/A converter, is designed to fill the performance requirements of arbitrary waveform generation in direct digital synthesis (DDS), waveform reconstruction in communications systems, and wide-range, high-speed A/D converter design.

Supporting update rates up to 40 MSPS, the AD768 offers 16-bit resolution with 1/2-LSB differential and 1-LSB integral nonlinearity at the 14-bit level, and low 35 pV-s glitch. On-chip features include edge-triggered CMOS latches for the digital interface and a 2.5-V reference (an external reference may be used). Complementary outputs can be used individually or differentially, to provide a 20-mA-full-scale current that settles to 0.025% within 25 ns. AC specified, the part will provide 1-MHz output with 83-dBc spurious-free dynamic range (SFDR).

The AD768 operates on ±5-V supplies, typically consuming 465 mW of power. It is available in a 28-pin SOIC package and is specified for operation from –40 to +85°C. An evaluation board is available. Prices are $24.95 for the AD768AR in 100s and $150 for an evaluation board.

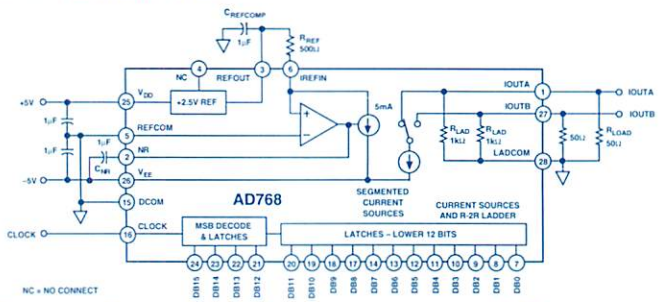


Figure 1. Functional block diagram of the AD768 and basic hookup.

A TYPICAL APPLICATION

Multitone transmitters (for ADSL): Communication applications frequently require aspects of component performance that differ significantly from the simple single-tone signals used in typical tests. This is especially true for spread-spectrum and frequency-division-multiplexed (FDM) signals, where information is contained in a number of small signal components spread across the frequency band. Such applications require a combination of wide dynamic range, good fine-scale linearity, and low intermodulation distortion (Figure 2). Full-scale SNR and THD performance alone may not reliably indicate how a device will perform in multitone applications.

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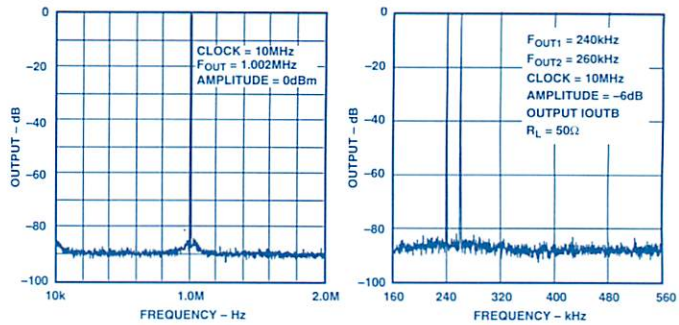


Figure 2. SFDR and 2-tone intermodulation distortion with 10-MHz clock.

The discrete multitone (DMT) asymmetrical digital subscriber line (ADSL) communication system standard, currently under consideration by ANSI, is a case in point. Figure 3 is a block diagram of a transmitter function. A set of discrete tones in the frequency domain are quadrature amplitude-modulated (QAM) digitally, and a 512-point inverse FFT transforms them into a time-domain signal at 2.2 MSPS. An FIR interpolation filter upsamples—in this case, to 4.4 MSPS, and a D/A converter (the AD768) converts to analog; the signal is smoothed and goes on to the transmitter.

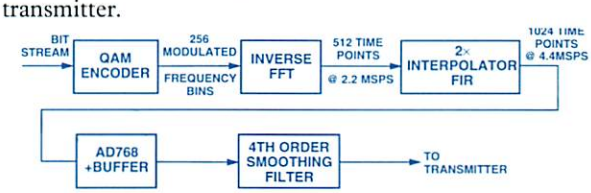


Figure 3. Typical discrete multitone ADSL Transmit chain.

Figure 4 shows a frequency-domain representation of a test vector run through the system and the corresponding time-domain representation (which looks a lot like noise). The signal-to-noise-and-distortion (SINAD) ratio of each 4-kHz component is a function of noise (wideband and quantization) and distortion (simple harmonic and intermodulation) in the DAC and filter. The AD768's combination of 16-bit dynamic range and 14-bit linearity provides excellent performance for the DMT signal. The tables below show the signal-to-noise ratio obtained at the output of the filter for various frequency bins in the ADSL application.

Frequency	SNR	Frequency	THD
151 kHz	63.5 dB	160 kHz	–60 dBc
349 kHz	65 dB	418 kHz	–53 dBc
500 kHz	64.8 dB	640 kHz	–57 dBc
1 MHz	61.9 dB	893 kHz	–57 dBc

The AD768 was designed by Doug Mercer, of ADI's Standard Linear Products Division, at our Wilmington, MA facility.

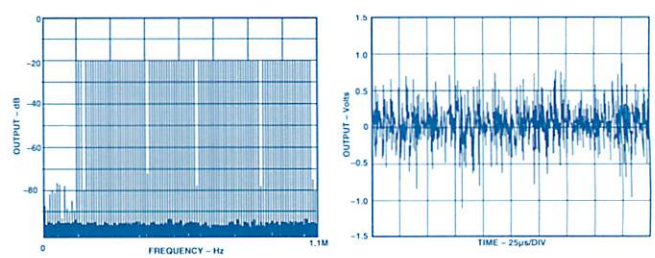


Figure 4. Output spectrum of ADSL test vector, and time-domain output signal.

12-Bit Dual DAC: Serial, Single Supply, Saves Space (SO-14)

+5-V-supply AD8522 includes 2.5-V reference and buffered voltage outputs. Surface-mount package is only 1.5 mm high

The AD8522* is a complete (Figure 1) dual 12-bit digital-to-analog converter (DAC). Low in cost and easy to use, it is available in a space-saving 1.5-mm-high 14-pin surface-mount (SO-14) package—as well as a 14-lead epoxy DIP—and requires no external components for operation.

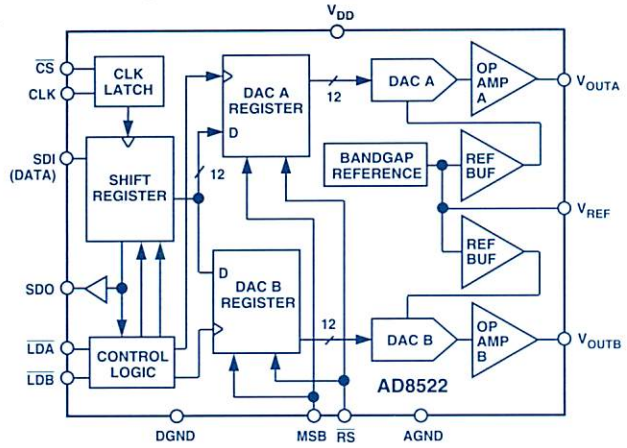


Figure 1. Functional block diagram.

Requiring only 5 mW of power quiescently (and 25 mW maximum, with TTL input levels) from a single +5-volt ±10% supply, it has monotonic output and a maximum integral nonlinearity (relative error) specification of ±1.5 LSB (±0.037% FSR) over its temperature range of –40 to +85°C (Figure 2), with a ±1-LSB match between the two channels. The AD8522 was designed for use in fixed and portable applications in equipment for digitally controlled calibration, and in dc setpoint applications for communications and process control. It is priced at $8.36 in 1000s.

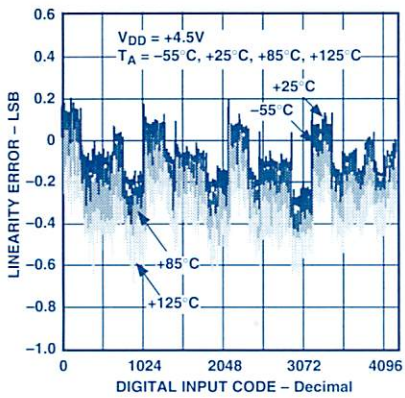


Figure 2. Typical linearity error plotted as a function of digital code and temperature.

*Use the reply card for technical data. Circle 6 (for sample—circle 47 and mention model no.)

The AD8522 includes a serial digital interface, an on-board 2.5-V bandgap reference, and buffered voltage outputs capable of driving ±5 mA at half-scale. Full-scale output is 4.096 V, set by laser-trimming (4.095 V for an input code of FFF_H), an easy-to-use 1.0 mV/LSB. Serial data can be clocked in at 14 MHz and more.

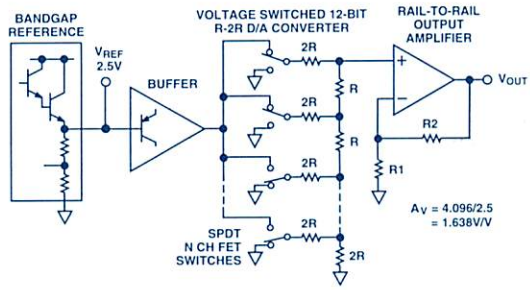


Figure 3. Equivalent schematic of analog portion of AD8522.

Figure 3 shows the analog portion of the AD8522, including the curvature-corrected bandgap reference—which can provide +2.5 V at up to +5 mA externally (0.5% regulation); the voltage-switched R-2R ladder, and the rail-to-rail output amplifier, with gain factory-set for the specified output range. DC specifications over temperature include ±1 LSB differential nonlinearity (monotonic), full scale voltage error ±16 mV (including the error of the internal voltage reference), with a tempco of ±15 ppm/°C.

The device's output can drive a 500-pF load without oscillation; output settling time is 16 µs to +FS ± 1 LSB, and to 0 + 6 LSB. Digital feedthrough is 2 nV-s, DAC glitch is 13 nV-s, and crosstalk is –38 dB while changing Load Enable in the opposite DAC.

Hardware and software modes: The AD8522 has a 16-bit serial input register that accepts clocked-in data when the CS pin is active low.The DAC registers are updated by the Load Enable ($\overline{LDA}$ and $\overline{LDB}$ pins). Data can be loaded into the DACs in either a hardware or a software mode.

Hardware load directs the data currently clocked into the serial shift register into the DAC A register, the DAC B register, or both, depending on the active-low strobing choice for the $\overline{LDA}$ and $\overline{LDB}$ pins. Software-hardware serial data-register bit, Sf/$\overline{Hd}$, must be low for this mode to be in effect (Figure 4).

Software load permits the number of control lines to the AD8522 to be minimized. In this mode of operation, with bit Sf/$\overline{Hd}$ high, the $\overline{LDA}$ and $\overline{LDB}$ pins act as one control input, taking the present contents of the serial input register and transferring the 12 bits of data into the decoded address determined by the address bits, A and B, in the serial input register.

The AD8522 was designed by Derek Bowers and Carol Flores at our Santa Clara, CA facility.

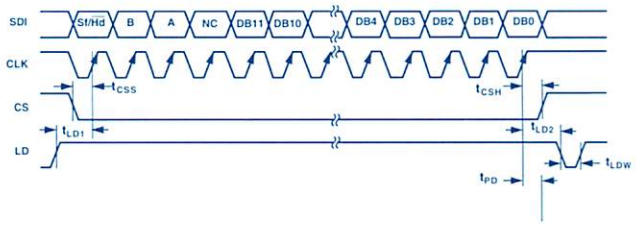


Figure 4. Timing diagram, showing software-control bits (Sf/$\overline{Hd}$, A, and B).

16-Bit Fixed-Point DSP with 80 KBytes of RAM Reduces System Cost

ADSP-2181 eases design of reprogrammable systems, has 2 serial ports, plus 8-bit & 16-bit parallel DMA ports

The ADSP-2181* is a 16-bit fixed-point reprogrammable digital signal processor (DSP) with 80 Kbytes of on-chip random-access memory (RAM), significantly more than is available on any other general-purpose fixed-point DSP. The fully integrated RAM and on-chip peripherals maximize on-chip performance, eliminating the need for external SRAM. This greatly reduces cost (the extra memory is essentially free in this competitively priced processor) and increases speed, since the additional lags inherent in using external buses are eliminated when communicating with on-chip memory.

Many complete applications can fit in the on-chip RAM, for example, high-speed data communications (V.32bis modems), spectrum analysis, speech compression (GSM, VSELP), or music synthesis. Because of download-ability, system-level designs requiring larger amounts of memory can use slower, low-cost byte-wide read-only memory (ROM) and host-system dynamic RAM instead of high-speed, expensive SRAM (Figure 1).

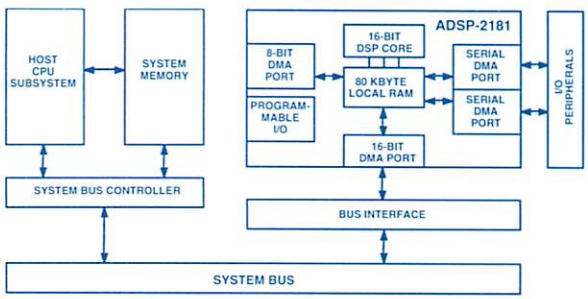
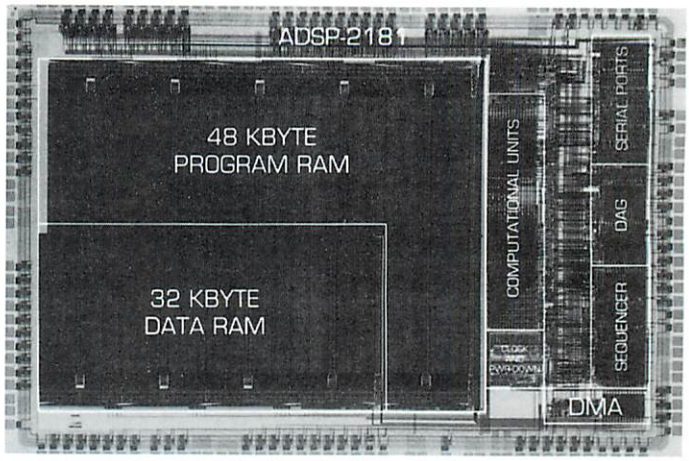


Figure 1. Typical system configuration.

In embedded systems, the 8-bit parallel direct memory-access (DMA) port allows simple interfacing to low-cost, byte-wide PROMs, EPROMs, and ROMs, for storage of large data tables and program overlays. In host-based, or multiple-processor systems, the 16-bit parallel DMA port provides a high-speed communications port to system buses, allowing the host—or other processor—to directly access the ADSP-2181's on-chip RAM. This capability facilitates on-the-fly configuration of the DSP for multiple applications.

With its combination of high performance and multiple data-I/O ports (Figure 2), the ADSP-2181 can be easily reconfigured to suit a variety of systems and applications—for example, in integrating audio, video, and communications software into the PC

*Use the reply card for technical data. **Circle** 7



environment. The key performance benchmarks shown below illustrate the ADSP-2181's capabilities in PC-based sound and communications applications; they compare quite favorably with the best performance of any general-purpose fixed-point DSP. The benchmarks are executed from on-chip memory; other DSPs require external high-speed SRAM, which typically hogs a large portion of the DSP subsystem cost and time budgets.

FFT:	
1-K point, complex, radix 4, DIF, FFT	1.07 ms
4-K point, complex, radix-4, DIT, FFT	5.5 ms
Voice, Data:	
20-voice synthesis	20 MIPS
11-voice emulation	16 MIPS
V.32bis (14.4 kbps)	16 MIPS
V.34 (28.8 kbps)	32 MIPS

The ADSP-2181 also provides a number of hardware- and software power-down modes, which allow the DSP to be placed in a "sleep" mode or in a reduced-power operating mode, to prolong battery life in portable applications.

For space-critical applications, such as portable communications and PCMCIA cards, the ADSP-2181 is available in a 128-lead PQFP (plastic quad flatpack) and a TQFP (thin quad flatpack)—which is just 1.4 mm thick. The device operates at 33 MIPS from a +5-V supply (3.3-V operation is also in the offing). As with all Analog Devices DSPs, there is a full suite of software and hardware tools for support. The ADSP-2181 in PQFP is priced at $51 in 1000s.

The ADSP-2181 was designed by a team led by Greg Koker at our Norwood MA facility.

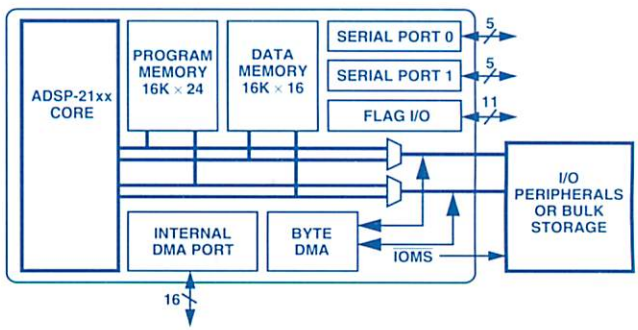


Figure 2. Block diagram of the ADSP-2181

Simple Techniques Protect Amplifiers from Input Overvoltage

First, understand how the amplifier behaves under fault conditions

by Joe Buxton

Common-mode overvoltage on the inputs is a potential problem in any analog measurement system that interfaces to the "outside" world. Op amps and instrumentation amplifiers often have the difficult job of interfacing to external signal sources, such as sensors or other electronics, which may expose the system to voltages that exceed the parts' absolute maximum ratings. For example, a fault condition, such as an accidental short to other circuitry or equipment, could cause the sensor and wires to contact high voltages and apply them to the sensor amplifier. Natural phenomena, such as thunderstorms, can also induce overvoltages.

Regardless of the cause, whenever the input voltage exceeds an op amp's ratings, it could be damaged, whether the device's power supplies are on or off. In fact, with power off, even small fault voltages can damage the device. For example, when an op amp operates on ±15-V supplies, the input's magnitude must exceed either +15 V or −15 V before damage can occur. But with the supplies turned off, voltages as small as ±0.7 V can cause damage. A typical instance where this kind of fault may occur is when interconnected circuits are powered separately—and one is turned on while the other is off. The live circuit can easily apply sufficient voltage to damage the ICs in the circuit that is off.

The best way to avoid damaging an amplifier is to eliminate all overvoltage conditions. However, predicting all possible fault conditions is a well nigh impossible task. Once an IC is damaged, it must be replaced (as well as any other devices that its failure caused to fail), a costly procedure when possible; But more often than not, the IC will be damaged in the field, resulting in costly re-working of the equipment (if it is recoverable). Thus, routinely designing to protect amplifiers from damage is an imperative for long-term reliability and low maintenance costs.

The first step in protecting an amplifier from overvoltages is to understand how it behaves when subjected to fault conditions. Once the failure mode has been determined, appropriate protection needs to be applied to the circuit—often as simple as adding a series input resistor or providing external clamping. Using fairly simple techniques, a designer can protect a circuit from overvoltages from a few volts to hundreds of volts, avoiding headaches and expense. But when external elements are added, their effects on the overall circuit performance must be considered.

Overvoltage can destroy an amplifier (gradually)

Given a high enough input voltage of the appropriate polarity, any op amp will conduct current to either the positive rail or the negative rail. While all op amps and instrumentation amplifiers are susceptible, the actual threshold for significant current flow differs appreciably for different devices. A typical conduction voltage can be as low as a diode drop of 0.6 V or as high as a process breakdown voltage of 50 V or more. The threshold for a particular amplifier depends on its input-stage architecture, as we will see.

Though popular opinion and most data sheet specs skirt this point, forward conduction of itself during an overvoltage is not inherently damaging to an IC unless accompanied by substantial current flow. Currents of 100 mA and more can quickly cause the input traces to burn out, resulting in a damaged part. But, if the current is limited to microamperes, or even a few milliamps, most amplifiers will be safe, even with continuous overvoltage. In fact, a simple resistor will generally protect an amplifier under almost all overvoltage conditions. But its presence degrades performance, so most amplifiers do not have inherent current limiting in their input stages. In those cases, when overvoltage does occur, unlimited current can flow and destroy the part.

The actual value of current that can damage an amplifier is a function of input stage construction, particularly, the width of the metal traces in the IC's input stage. A phenomenon known as *metal migration* occurs whenever the current density within a metal trace exceeds a certain level—about 1 mA per 1 µm of width for a typical 1-µm-thick trace. Thus, for a 5-µm-wide metal trace, the maximum safe current is about 5 mA. Beyond this level, atoms of the metal begin to move. In time, enough metal can migrate to cause an open circuit in the trace (and a bulge elsewhere), rendering the part inoperable. Input trace widths do differ from amplifier to amplifier, usually in the 5-to-10-µm range. There are exceptions, but for most bipolar parts, limiting the input current to less than 5 mA protects the device. This assumption is maintained in the following discussion.

An IC can often be subjected to more than 5 mA and still appear to function normally. But this does not guarantee that the part is free from damage. Metal migration is a *cumulative* effect; it may take a long time to cause a failure. But the damage will build up, eventually resulting in an open trace here or a short-circuit there. Such failures due to repeated overvoltage are difficult to detect in the early stages. The more current that flows during an overvoltage, the more the migration accelerates, and the sooner an open trace results. So, even though an amplifier may appear to withstand overvoltage currents well above 5 mA for a short time, it is important to observe the 5 mA limit to improve the prospect of long-term reliability.

Factors affecting amplifier overvoltage characteristics: Two methods of conduction occur in overvoltage conditions: forward biasing of PN junctions inherent in the structure of the input stage and—given enough voltage—reverse-bias junction breakdown. The only danger of forward biasing a PN-junction is that excessive current would flow and damage the part. As long as the current is limited no damage should occur. However, when the conduction is due to the reverse bias breakdown of a PN junction, the problem can be more serious, depending on the junction in question. For the case of a base-emitter junction breaking down, even small amounts of current can cause a large degradation in the forward beta of the transistor.[1] After a breakdown occurs, the input parameters of the op amp, such as offset and bias current, may degrade well beyond the specified values. External diode

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[1] *Analog Integrated Circuits*, Paul R. Gray and Robert G. Meyer, J. Wiley and Sons, 1984, page 28.

protection (to be discussed) is needed to limit voltage to prevent base-emitter junction breakdown.

The structure of the input stage affects the overvoltage characteristics of an amplifier. Many paths may exist in an amplifier to form a diode to either the positive or negative supply. For example, many bipolar devices are built on a substrate made of *p*-type silicon, which is electrically connected to the negative supply. This *p*-type material forms "substrate" diodes in conjunction with various *n*-type structures in the IC's circuitry. When the input goes below the negative supply, a substrate diode may clamp the input to within 0.7 V of the negative supply. The substrate diodes typically have low resistance, so virtually unlimited amounts of current can flow until the part is destroyed. The next section describes in detail a few of these structures that lead to PN junctions energizing during an overvoltage condition.

The overvoltage characteristics of an amplifier are not often apparent just from the data sheet. Input stages differ widely resulting in a variety of overvoltage characteristics. The simplified schematics in data sheets can sometimes suggest paths of forward biasing PN junctions. More often, though, there is not enough information to determine the overvoltage characteristics. Indeed, a full schematic with the process cross section is needed, and it should be interpreted by one wise to the ways of IC circuitry. Even then, possible conduction paths are not always apparent. In cases

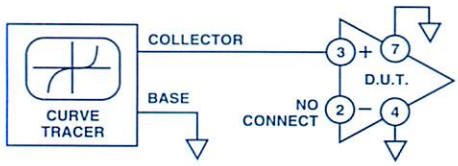


Figure 1. A curve tracer can be used to quickly determine the overvoltage characteristic of an amplifier.

where no obvious path exists, or the schematic does not contain enough detail, (and perhaps as a general rule) one's best route is to measure an amplifier's characteristics in the lab.

A curve tracer can be quickly configured to measure the overvoltage characteristics of any amplifier, as shown in Figure 1. The curve tracer ramps a dc voltage on the input and measures the current flowing into or out of the input stage. For most amplifiers, having symmetrical inputs, this measurement yields the same results, independently of which input is measured. Current feedback amplifiers are an exception to this rule; their positive and negative inputs have different characteristics. If a curve tracer is not available, similar results can be obtained in a short time using a dc voltage source and a multimeter; connect the source to the input through a 10-kΩ resistor, and measure the current as a function of the input voltage.

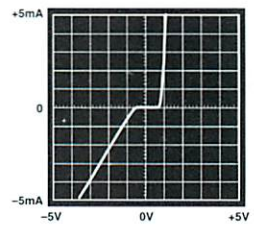
The supply voltages can be configured as desired; for simplicity, all the measurements in this article were made with both supplies connected to ground. The state of the other input is an important consideration in determining the characteristics. Many amplifiers have input protection diodes connected across the differential input pair to prevent large *differential* voltages from damaging the input transistors by reverse biasing their base-emitter junctions; but they do not protect against large common-mode voltages. When measuring the overvoltage characteristics, the other input should be left floating to ensure that the input diodes do not conduct, thus concealing the characteristics of interest.

As noted above, amplifiers exhibit two basic types of overvoltage characteristics; recognizing the difference between the two on a curve tracer is important in understanding how to protect an amplifier. The forward biasing of PN junctions is evident because, as the input voltage rises above the supplies, distinct break points are encountered when internal diodes turn on. In most cases, this characteristic occurs within one or two diode drops of either supply. With forward conduction, simple current-limiting protects the amplifier. On the other hand, reverse-junction breakdown typically occurs only when the input rises at least 5 V above the positive supply or below the negative supply. The actual voltage for breakdown varies widely [in the OP42 example (Figure 3), it can be 50 V and more]. In such cases, an external diode clamp should be used to prevent breakdown.

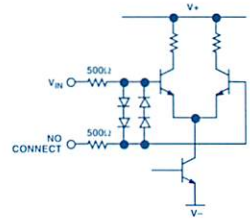
Two examples of overvoltage characteristics: Two amplifiers' overvoltage characteristics are shown here to illustrate how overvoltage characteristics can occur. This is certainly not an exhaustive cross section of amplifiers. Any different amplifier architectures should be checked individually.

Figure 2a shows the overvoltage characteristic of an OP177 precision amplifier. Because of its low offset and drift characteristics, the OP177 is commonly used to amplify low level sensor outputs. Thus, the OP177 could easily find itself in a circuit (especially with remote sensors) where overvoltage is likely. The curve tracer plot in Figure 2a shows that conduction is visible when the input exceeds the positive supply by about 0.6 V or goes below the negative supply by the same amount. Notice that in the positive direction the current quickly exceeds the 5-mA limit. However, in the negative direction, the current appears to be limited by a linear resistance. The reason can be seen when the input stage circuitry is examined in detail.

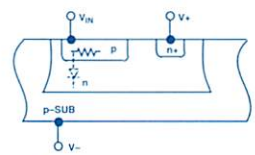
The input stage schematic in Figure 2b reveals a 500-Ω resistor in series with each input; this explains the current limiting in the *negative* direction. In fact, the curve shows a 4-mA change in input current for a 2-V change in input voltage, resulting in the expected 500-Ω slope. But, *what happened to the resistor for positive overvoltages?* The unlimited current flow rules out a series resistor. Also, where can we find the forward-biased diodes implied by the plot? To understand this, we need to examine the cross section of the process for the input devices. The input resistors are diffused



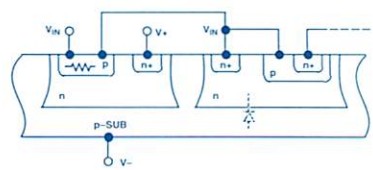
a. Measured characteristic using curve tracer.



b. OP177 input stage schematic.



c. Cross section, V_{IN} > V+.



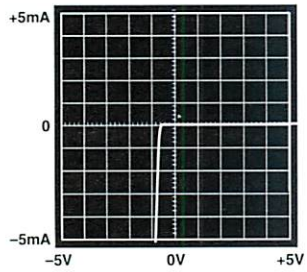
d. Cross section, V_{IN} < V–.

Figure 2. OP177 and overvoltage.

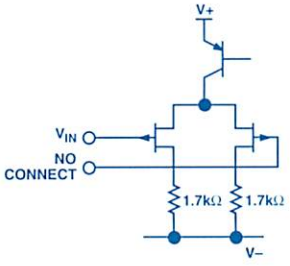
p-type material in a reverse biased *n* well, and the *n* well is electrically connected to V+, as shown in Figure 2c. When the input rises above V+, the junction between the *p*-type resistor and the *n* well forward biases, (dashed-line diode). Because the *p*-type material forward biases, the resistor is bypassed. In this case, essentially unlimited current can flow to the positive supply, causing the input stage to be damaged.

The conduction path in the negative direction is a little more complicated, but it can be identified by examining the cross section of the input devices. Figure 2d shows the same diffused resistor in series with one of the input protection diodes. For simplicity, the cross section of only one of the differential protection diodes (2b) is shown in (2d). As shown, these diodes are actually fabricated from NPN transistors, with the base-collector junctions tied together by a metal trace. The substrate of the entire chip is made of *p*-type silicon that is electrically connected to the negative supply. When the input drops below the negative supply, the input resistor and protection diode are pulled down. At 0.6 V below V–, the substrate to "collector" junction forms a diode, shown by the dashed line. The anode is the *p*-type substrate and the cathode the *n* well of the input protection diode. In this case, the *p*-type diffused resistor does not forward bias, so the resistance remains in series with the input to limit the current. Because only PN junctions forward bias when the input exceeds either supply of the OP177, the input current needs only to be limited to less than 5 mA to protect the device, and no external clamping is required.

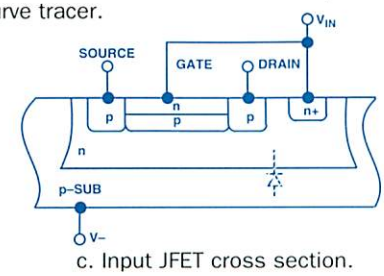
Figure 3 describes another typical input stage using a *p*-channel JFET differential pair. The OP42 is used as an example, but other JFET input devices behave in the same way. The curve-tracer response in Figure 3a shows an overvoltage characteristic very different from that of Figure 2a. For positive overvoltage, there doesn't seem to be a conduction path, but if higher voltage is applied, the input stage of the OP42 eventually breaks down at about 50 V. However, *negative* overvoltage quickly forward-biases an internal diode that can conduct large amounts of current. The input-stage schematic (3b) shows the differential *p*-channel JFET with no input series resistance or protection diodes but provides no clues as to how conduction occurs. Again, one can find the conduction paths in the input cross-section.



a. Measured characteristic using curve tracer.



b. OP42 input stage schematic.



c. Input JFET cross section.

Figure 3. OP42 and overvoltage.

The *p*-channel JFET is an ion-implanted device built in *n* epi material, as shown in Figure 3c. The *n*-type gate and the *n* epi material are connected directly to the input. When the input voltage drops below the substrate potential (connected to V–), the substrate-to-*n*-well junction forward biases, forming a diode from the negative supply directly to the input. Because the silicon has low resistivity and no series resistor exists, essentially unlimited current flows. However, when a positive overvoltage is applied to the inputs, the *n* well and *n* gate are pulled above V+. Thus, the PN junctions (formed by the gate to drain and *n* well to substrate) in the input stage are reverse-biased and no conduction occurs—until eventually the input junctions break down if the input voltage is increased sufficiently—to about 50 V for the process on which the OP42 is fabricated. This breakdown, unlike base-emitter breakdown, is not inherently damaging to the JFETs if the input current is limited to <5 mA. However, as additional insurance, external clamping using a diode is recommended if the input voltage is likely to approach the breakdown region.

Externally protecting an amplifier: Op amps used in environments where overvoltages are expected require protection. Most amplifier types (except for the few with internal protection) require external resistors and, in some cases, diodes. For amplifiers with internal PN junctions that forward-bias whenever the input voltage exceeds the rail, the only protection needed is an external series resistor to limit the current to 5 mA. When reverse-bias junction breakdown is involved, external diodes are needed. Usually, the breakdown involves just one of the supplies, so only one diode is needed, with its current-limiting series resistor. When in doubt about an amplifier type's failure modes, check it out on a curve tracer. A simple 5-minute measurement can avoid the headaches of replacing failed amplifiers in the field.

Figure 4 shows the OP177's breakdown with added protection; it compares with the unprotected case in Figure 2a, where the current quickly exceeds 5 mA with an input only 1 V above the positive supply. With a 2-kΩ resistor in series with the input, the current is now limited to 5 mA for input voltages up to 10 V beyond the supply voltages. The equation for picking the value of series resistance is very simple. Just divide the magnitude of maximum expected overvoltage (positive or negative) by 5 mA. In this test, the op amp's positive input is the only one connected to the outside world, so no protection is needed for the negative input. However, in cases where both inputs may be subjected to overvoltage—as in differential configurations or instrumentation amplifiers—both inputs require protection.

Whenever components are added, the circuit needs to be analyzed to determine the effects of adding them. Here, the series protection resistor adds to the offset and noise of the circuit. The offset is simply the product of the bias current and resistance; in

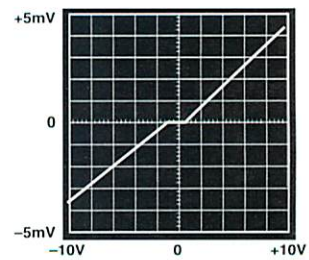
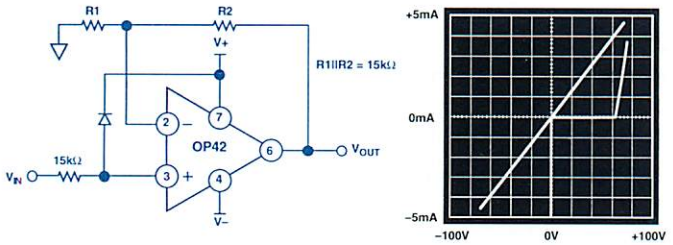


Figure 4. OP-177 input current, using protective resistor.

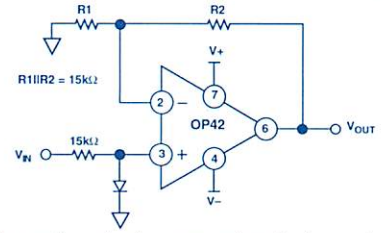
balanced amplifiers, the offset can be minimized by equalizing resistances seen by both inputs. The thermal noise contributed by the resistor, and the voltage developed by the amplifier's current noise flowing through that resistor, combine with the voltage noise of the op amp as root-sum-of-the squares (rss). If either of these error contributions is unacceptably large, a possible alternative is to add clamping diodes from the input to both supplies. If the diodes can handle currents >5 mA, the series resistance can be reduced. The diodes and resistor should be selected such that the external diode turns on at <0.6 V for the maximum overvoltage, to avoid turning on the internal diodes. However, external diodes may in some cases cause problems of their own, as will be seen below.

When the overvoltage characteristic of an amplifier shows breakdown occurring, external clamp diodes should be added to prevent the amplifier's input voltage from ever reaching that breakdown voltage. Often, breakdown occurs in only one direction and requires only one external diode for adequate protection. This helps keep the parts count down and minimize the diode's parasitic effects. In either case, a series resistor is still needed to limit the current through the amplifier. The OP42, with its 50-V positive breakdown, is used as an example in Figure 5a. Here, a diode has its anode connected to the input and its cathode to the positive supply. When the input exceeds the positive supply by approximately 0.6 V, the diode forward-biases and limits the input voltage to well below the breakdown voltage, whether or not the part is powered on. A series resistor is included to limit the currents through the diode and the amplifier for negative overvoltages. In this example, for a maximum input voltage of ±75 V, a 15-kΩ resistor is required to limit the current to 5 mA. As the curve tracer shows in 5b, the clamp diode turns on when the input exceeds V+ by 0.6V, and the series resistor limits current in both directions.



a. Reversed diode connected to V+.

b. OP42 with and without over-voltage protection.



c. Alternative diode connection for lower leakage.

Figure 5. Diode protection of OP42.

In high-impedance applications, the choice of diode is critical because it adds to leakage current. The diode chosen will depend on the maximum leakage-current requirement. A common 1N914 or 1N4148 diode typically has 10 nA of leakage. This is certainly not a very good choice to use with a JFET amplifier in a low-bias-current application, but may be adequate for less demanding applications. A good intermediate choice for a protection diode is the base-collector junction of a 2N3906 transistor. The transistor is a low-cost part with leakage currents of the order of 10 pA. For the most demanding applications, low leakage FETs may be required. Such parts as the 2N4117A and PAD1, from Siliconix, provide protection with leakage currents under 1 pA. However, when JFET protection diodes are used for their low leakage, the temperature effects must also be considered. JFETs typically exhibit a doubling of leakage current for every 10°C temperature rise. This rise must be compared to the op amp's bias current characteristic over the full operating temperature range of the circuit. With a JFET input amplifier, which has similar temperature behavior, the diode's leakage may still be less than the amplifier's; in some cases, the 2N3906 may be the better choice.

In applications where small negative (and even smaller positive) voltages must be measured at high impedance, Figure 5c shows an alternative configuration for connecting the diode. Here, the anode is connected to the input, so that the diode conducts for positive input voltages, but the configuration offers especially low leakage for small negative input voltages, because the reverse bias voltage on the diode is only $-V_{IN}$, instead of $-V_{IN} + V^+$. This configuration may also be useful for high-impedance measurement of small positive voltages (well below 50 mV). However, if the input goes more than 50 mV above ground during normal operation, the diode slowly starts to forward bias, the leakage goes up, and response to large inputs becomes nonlinear. The choice between protection schemes depends entirely upon the application and the expected voltages.

The amplifiers discussed above do not have internal overvoltage protection, except possibly for differential-input protection. However, there exists a small group of amplifiers that are designed to handle input voltages that exceed the supplies.* Such amplifiers often use thin-film resistors in series with both inputs to limit fault current. They, unlike diffused resistors, are isolated from the silicon by silicon dioxide, do not form a diode to either supply, and thus can limit current like external resistors. For example, the OP90, with 4-kΩ thin-film resistors, is guaranteed to handle voltages of magnitude up to 20 V greater than either supply. Another method is to use protection JFETs in the input stage; they turn on during an overvoltage condition and shunt current to the supplies. The AMP-02 instrumentation amplifier, using this scheme, allows its inputs to reach 60 V without damage. The designer should check a part's Absolute Maximum rating to determine its capabilities. For most amplifiers, that rating will read: "$\pm V_S$". To maximize the performance in benign environments, such amplifiers do not have protection on-chip, so external protection is needed. But the ability of amplifiers with protection to handle higher voltages is specified on the data sheet.

Summary: Input overvoltage, a common problem, requires careful design practice to avoid damaging amplifiers. Consider the environment that a particular amplifier is required to operate in and identify any possible overvoltage modes. Once the voltage levels are established, the op amp must be investigated to see how it behaves under these stress levels. Then the appropriate protection, if required, must be included. An ounce of prevention at the design stage will forestall headaches in the field.

*Examples: Operational amplifiers such as the AD820, AD822, OP90, OP290, OP291, OP490—and instrumentation amplifiers, such as the AD524, AD626, and AMP02. For technical data on these amplifiers, **Circle 8**

Amplifiers: Transimpedance, Isolation, μPower, VCAs

Quad VCA for Audio

SSM2164 has 0.02% THD, −100 dB ≤ Gain ≤ +20 dB

The SSM2164 has four independent channels of voltage-controlled current gain with an adjustment range of 120 dB and a gain sensitivity of −33 mV/dB for each channel. The channels are matched to within 0.07 dB at unity gain, with a low 0.02% 2nd and 3rd-harmonic distortion (0.1% max). A single resistor establishes Class A or Class AB operation.

Housed in a 16-pin plastic DIP or narrow SO package, and requiring no external trims, the SSM-2164 provides economy of space and cost per channel in multi-adjustment audio systems. Typical applications include remote, automatic, or computer control of volume, balance, or fade in mixers, compressors, limiters companders, sound processors, Surround Sound, and spatial-effect generators. The operating temperature range is −40 to +85°C. Price is $2.50 in 1000s. **Circle 9**

TransZ Amp

240-MHz AD8015 has Differential outputs, low cost

The AD8015 is a low-noise, wideband current-input, differential-voltage-output transimpedance amplifier designed for use in fiberoptic serial data systems. It is a complete single-chip solution for converting photodiode current into a differential, ECL-compatible voltage output. Its 240-MHz bandwidth makes it useful in FDDI receivers and SONET/SDH receivers with data rates up to 155 Mbps.

A low-cost silicon alternative to GaAs-based transimpedance amplifiers, it is ideal for use in systems requiring a wide-dynamic-range preamplifier or single-ended to differential conversion.

Specs include 1.5-ns rise and fall times, 2-pA/$\sqrt{\text{Hz}}$ current noise at 100 MHz, low power (25 mA at +5-V), and −40 to +85°C operation. It is available in an 8-pin plastic SOIC or in chip form. Prices start at $3.59 in 1000s. **Circle 11**

Input Isolation Amps

2-port AD102/AD104 have ±0.05% max nonlinearity

The AD102 and AD104 2-port isolation amplifiers provide a complete solution for applications requiring 500-V rms input isolation with >100 dB of common-mode rejection. Transformer-coupling provides an integral isolated front-end power supply for its galvanically isolated input amplifier, an uncommitted op amp that can provide gains up to 100 V/V.

The **AD102**, with 1.5-kHz full-power −3-dB BW, requires +15 V dc (75 mW) and no external components to operate; the **AD104,** with 4-kHz BW, calls for a 25-kHz 15-volt (35 mW) square-wave clock source. The AD104 is especially useful in multi-channel systems requiring input-to-input isolation. Both devices use a small-footprint 2.08"×0.260"×0.625" max, SIP-style package, and operate from −40 to +85°C, with performance specified from 0 to +70°C. The AD102/104 are priced at $24/$22.50 in 100s). **Circle 13**

Trimless VCAs

SSM2018T & SSM2118T: V & ΔI out, 0.006% THD+N

The SSM2018T and SSM2118T are high-performance voltage-controlled amplifiers pretrimmed for minimum distortion for use in professional audio equipment, such as audio processing, mixing consoles, and noise-reduction systems. The **SSM2018T** has voltage output, and the **SSM2118T** has differential current outputs for ease in low-noise summing of multiple outputs in large VCA-based systems.

Both devices have differential voltage inputs and a 140-dB range of gain adjustment (+40 to −100 dB), 0.006%THD+N (1 kHz, unity gain), and a 117-dB dynamic range. The buffered control port has −30 mV/dB sensitivity. The maximum power-supply current is 15 mA with ±15-volt supplies; operating temperature range is −40 to +85°C, and the devices are packaged in 16-pin plastic DIPs and SOLs. Prices begin at $3.00 in 1000s. **Circle 10**

Single-Supply OA

Rail-to-Rail input & output OP191: +3 to +10-V supplies

The OP191 is a single version of the dual and quad OP291/OP491 introduced here in vol. 28-2 (p.21). A single-supply amplifier, its output can sink and source current, and swing to within a few millivolts of the supply rails (V^+ − 5 mV min and V^- + 10 mV max with 100 kΩ load to opposite supply terminal); and its input can actually swing safely 10 volts beyond either supply without phase inversion or latchup.

With a 16-V absolute max specification, the OP191 is specified for operation with +3, +5, and ±5 V supplies. Drawing ≤0.5 mA (−40 to +125°C) from a 3.0-V supply, the device has a gain-bandwidth product of 3 MHz, full-power bandwidth (1% distortion) of 1.2 kHz, and 0.4 V/μs slew rate (10-kΩ load). It is available in an 8-lead narrow-body SO or an 8-lead epoxy DIP. Price is only $1.67 (1000s). **Circle 12**

Rail-to-Rail, High I_{out}

OP279 is a dual 50-mA Op amp for +5-V systems

The OP279 is a monolithic op-amp pair that can handle rail-to-rail input and output swings, and sink and source 50-mA output current (up to 80 mA, short-circuit). With a 4.5-to-12-V supply range, it is specified for operation at +5 V and ±5 V, at temperatures from −40 to +85°C. Maximum supply current at +5-V is 3.5 mA per channel. Applications include driving headphones on sound cards, modem transformers, and cables.

It will also provide rail-to-rail buffering with more power than CMOS. Typical specs include low distortion (0.01% with 600-Ω load), low noise (21 nV/$\sqrt{\text{Hz}}$), wide bandwidth (5 MHz), high slew rate (3 V/μs). It is unity-gain stable, and will not reverse phase with overdrive. Its output can drive 10 nF capacitance stably. It is packaged in 8-lead narrow-body SO and 8-lead epoxy DIPs. Price is $1.31 in 1000s. **Circle 14**

Interfaces: RS-232, RGB→NTSC/PAL

3.3-V Drive/Receive

For true RS-232 at low cost & Ultralow power: ADM560/61

The ADM560 and ADM561 contain 4 drivers and 5 receivers designed to meet EIA-232 standards while operating with a single 3.3-V supply. Consuming only 5 mW, an on-chip dc-dc converter, including a voltage doubler and inverter, generates ±6.6 V to operate the interfaces. A shutdown facility further reduces the power to *0.66 μW*. A pin-compatible upgrade for other 560/561s, applications include battery operated equipment, such as laptops, palmtops, notebooks, etc.

They differ mainly in polarity of control logic for receiver Enable and Shutdown. Features include operation with +3-V or +5-V logic and a 116-kbit/s data rate. Two receivers remain active in shutdown (ADM560) for monitoring wake-up calls. Available in 28-pin SO and SSOP, they operate from 0 to 70°C and require 1-μF external capacitors. Prices start at $2.18 in 1000s. **Circle 15**

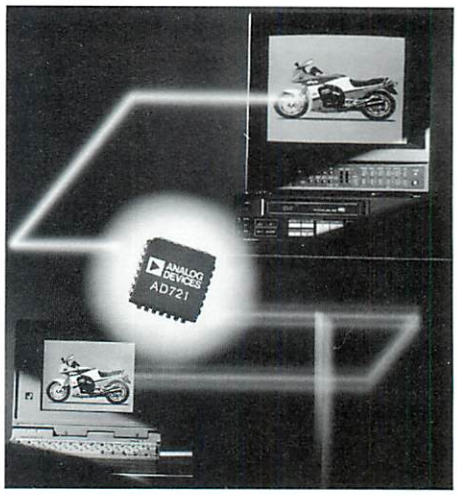
Integrated RGB-to-NTSC/PAL Encoder

AD721 includes pin-selectable ENCODE/By-Pass mode, Has on-Chip Triple Buffer to Drive RGB Monitor directly

The AD721 high-picture-quality RGB-to-NTSC/PAL analog encoder is the industry's first to integrate a pin-selectable ENCODE/By-Pass mode and triple buffer amplifiers for directly driving RGB monitors. On-chip 100-MHz gain-of-2 video amplifiers easily drives 75-Ω reverse-terminated loads.

The AD721 encodes red, green, and blue (RGB) component video signals into NTSC or PAL luminance (baseband amplitude), chrominance (subcarrier amplitude and phase), and composite (S-Video) video signals. No external filters or delay lines are required. The AD721 also features a Bypass mode, for bypassing the encoding.

Like the encoding-only AD720 (*Analog Dialogue* 27-2, p. 27), the AD721 provides a complete, fully calibrated function, requiring only termination resistors, bypass capacitors, a clock input at 4× the subcarrier frequency, and a composite sync pulse. There are two control inputs; one selects the



TV standard (NTSC/PAL) and the other activates the triple bypass buffer to drive the RGB signals when encoding is not required. The device, in a compact 28-pin PLCC, uses a ±5-V supply. It is priced at $6.15 in 10,000s. **Circle 17**

Multiple Interface

+5-V ADM223 has 4 RS-232 Drivers and 5 receivers

The ADM223 has a set of 4 drivers and 5 receivers intended for all EIA-232-E and V.28 communications interfaces; it requires just a single +5-V-supply. A low-power shutdown mode reduces power dissipation to less than 5 μW, making it ideal for battery-powered equipment. It is similar to the AD241L (A-D 28-1, p. 25), but has complementary receiver control logic; unlike ADM241L, receivers R4 & R5 can remain enabled in shutdown, allowing them to detect a wakeup signal.

The ADM223, an upgrading replacement for other 223-type interfaces in applications requiring high mouse-drive current, includes two internal charge-pump voltage converters, using 1-μF capacitors. It accepts a 120-kB/s data rate and ±30-V receiver inputs, is housed in 28-lead SOIC and SSOP, and is rated for –40 to +85°C. Prices start at $1.85 in 1000s. **Circle 16**

RS-232 Interface

+5-V ADM203 requires *No external capacitors*

The ADM203 has 2 drivers and 2 receivers that meet EIA-232-E and V.28 specifications. It operates from a single +5-volt supply and generates internally the required ±10 volts. Its efficient charge-pump design permits the capacitors to be included within the package, so no external capacitors are required. Its low-power latchup-free BiCMOS process results in a power requirement of only 2.0 mA at +5 V (10 mW).

Fast driver slew rates enable it to handle a 120-kb/s transmission rate, and its receivers will withstand continuous voltages in excess of ±30 V. A pin-compatible upgrade for other 203 types, its typical applications include computers, modems, peripherals, etc. The ADM203 is housed in a 20-pin DIP package and operates at temperatures from 0 to 70°C. It is priced at $2.76 in 1000s. **Circle 18**

RS-232, 0.1-μF Caps

+5-V driver/receiver family ADM205-211 & ADM213

The ADM205-211 and ADM213 (pin-compatible upgrades for industry standard types) combine various numbers of line drivers/receivers (see table) for EIA-232-E and V.28 communications interfaces. All the devices operate with +5-V supplies; the ADM209 also requires +12 V. They use space-saving 0.1-μF external capacitors (except for ADM205, with self-contained capacitors). The devices indicated can be shut down to save power (≤5 μW); two of the ADM213's receivers remain active during shutdown. The devices are variously available in DIPS, SOICs and SSOPs. Prices (1000s) start at $1.85 (ADM211AR). **Circle 19**

DEVICE COMPARISON

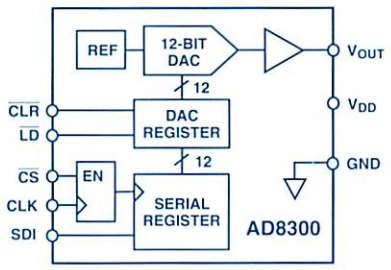
	ADM205	206	207	208	209	211	213
Drivers	5	4	5	4	3	4	4
Receivers	5	3	3	4	5	5	5
External caps.	0	4	4	4	2	4	4
Shutdown?	√	√				√	√
TTL 3-state $\overline{EN}$	√	√			√	√	√

A/D and D/A Converters

+3-V Serial-Input Complete 12-Bit DAC

Space-saving AD8300 in SO-8 has smallest footprint Rail-to-rail, monotonic, no trims necessary, 3.6 mW

The AD8300 is a +3-V single-supply, complete 12-bit D/A converter in a space-saving SO-8 surface-mount package. Included on-chip with the DAC are an internal reference, output buffer amplifier, serial register, DAC register, and control logic. The device is laser-trimmed for a scale factor of 0.5 mV/bit (2.0475 V for full scale data = FFF_H) and it provides monotonic response (DNL <±1 LSB) with supply voltages from +2.7 V to +5.5 V over the –40 to +85°C range.



Consuming 3.6 mW typical (5.1 max), it offers significant power savings in battery-powered applications. For example, it can operate on a single-cell Lithium battery (2.8-V end-of-life). Its double-buffered serial input is efficient in terms of connections and real estate; and its fast loading rate of 12.5 MHz permits the bus to be freed quickly, whereas the DAC can be updated asynchronously. Its slew rate is typically 2 V/µs; it settles to within ±1 LSB of full scale and to within 3 mV of 0 in 14 µs.

The AD8300's integral nonlinearity error is pretrimmed to a maximum ±2 LSB, and its temperature coefficient of full-scale error is typically 16 ppm/°C. Its output amplifier will source 5 mA and sink 2 mA at half-scale (2.5-mV ΔV_{out}), and it can drive 500 pF without oscillation. It is available in 8-pin plastic DIP and SO. Its 1000s price is $4.46. For technical data, **Circle 20***

12-Bit M-DACs

AD7943/45/48 operate on Single +3.3/+5-V supply

The AD7943/45/48 are fast 12-bit current-output multiplying D/A converters that can operate on +5 and +3.3-V single supplies. They differ only in the way they accept data: the **AD7943** has a double-buffered serial interface; the **AD7948** has a double-buffered 8-bit byte interface; and the **AD7945**'s is 12-bit parallel. The AD7943 is available in 16-pin DIP and SO, the AD7945 and A7948 are available in 20-pin DIP and SO—and all three are available in 20-pin SSOP.

They are pin-compatible in +5-V designs that use industry-standard AD7543/45/48 but have greater speed (600 ns settling to 0.01%), require considerably less power (typically 5 µW), are also available in tiny SSOP packages, and they cost less. They feature ±0.5-LSB max differential and integral nonlinearity and are monotonic over temperature (–40 to +85°C). Price in 1000s is $3.95. For technical data, **Circle 23***

12-Bit Quad M-DAC

Single-supply AD7564 for +5/+3.3 V, serial interface

The AD7564 comprises four double-buffered serial-input, current-output 12-bit multiplying DACs in a single 28-lead DIP, SO, or SSOP package. Each DAC has an independent reference input and can be used for 4-quadrant multiplication.

The AD7564 can operate on a single +5- or +3.3-V supply, with guaranteed specifications, including all grades monotonic over temperature (–40 to +85°C). Data is clocked in (and out) serially, and the on-chip DACs are individually addressable. They can be simultaneously updated or cleared, using asynchronous $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ inputs.

The AD7564 is a low-power device, dissipating only 50 µW max at +5 V and 33 µW max at 3.3 V, making it ideal for multichannel portable instrumentation. Price is $11.90 in 1000s (less than $3.00/channel). **Circle 21**

12-Bit ADC: 8-pin SO

Single-supply AD7896; Rail-Rail inputs; Serial interface

The AD7896, a fast 12-bit sampling A/D converter, operates from a single supply (+2.7 V to +5.5 V) and converts with throughput rates up to 100 kHz min. It is complete in a single 8-lead mini-DIP or SO package (–40 to +85°C), including a track-hold, converter, control logic, and a high-speed serial interface. It accepts rail-to-rail inputs, from 0 V up to the supply, V_{DD}—which provides the reference.

Two operating modes are available. In Mode 1 (continuous operation), conversions occur in 8 µs (average power 9 mW at 2.7 V); in Mode 2, the device goes into a low-power "sleep" mode after a conversion, until the next Convert Start pulse is received—conversion time is about 14-µs (200 µW used at 1 ksps).

Two grades (A, B) are available for –40 to +85°C, plus an S grade—in Cerdip—for –55 to +125°C. Prices start at $6.75 in 1000s. For technical data, **Circle 22***

12-Bit 600-ksps A/D

+5-V Supply, 60-mW AD7892 Serial or parallel interface

The AD7892 is a complete cost-effective and versatile 12-bit sampling A/D converter, operating on a single +5-V supply, with a 600-ksps conversion rate, low power consumption (60 mW), and serial and parallel interfaces for flexibility. A 5-mW Standby mode further reduces dissipation. Included on chip are a 2.5-V bandgap reference, track/hold, plus the converter, control logic, and interfaces. The 12-bit parallel interface has a fast 35-ns bus access time, and the serial interface can be clocked at up to 20 MHz.

Three versions provide a selection of input ranges: ±5 V & ±10 V (AD7892-1), 0 to 2.5 V (-2), and ±2.5 V (-3). Versions -1 and -3 can withstand ±17 V and ±7 V, respectively. A and B grades operate at –40 to +85°C and are housed in 24-pin plastic DIP and SO packages. An S version will be available soon. Prices start at $12.75 (1000s). For technical data, **Circle 24***

**For a sample of any of these devices, Circle 47 and indicate the desired Model.*

Switches, Voltage References, Motion Control

Precision Switch

ADG417, SPST, in SO-8 has Rail-to-rail signal range

The ADG417, an upgrade of the industry-standard DG417 single-pole, single-throw switch, is available in 8-pin DIP and SO packages. The switch is ON for logic 0, OFF for logic 1. The ADG417 can be used with either single or dual supplies, with performance specified for ±15-V and +12-V supplies (and +5-V logic); it will work with a +5-V supply.

The ADG417's trench-isolated linear-compatible CMOS process (LC^2MOS) provides low power dissipation (<35 µW), fast switching (t_{ON}/t_{OFF} = 145/100 ns max), low *on* resistance (<35 Ω), and low leakage currents (±5 nA max, –40 to +85°C, ≤0.4 nA max at 25°C). Trench isolation gives all the benefits of dielectric isolation and ensures no latchup, even under severe overvoltage conditions. The signal range extends to the supply rails. Price (100s) is $1.20 (either package). **Circle 25**

Vector Rotation

AD2S105 resolves 3-phase Into orthogonal magnitudes

The AD2S105 Three-Phase Current Conditioner, a monolithic mixed-signal processor, performs vector rotations of three-phase signals using digitally supplied angular information. It computes the 90° orthogonal components of a 3-phase input, then transforms them to a new reference frame, controlled by the 12-bit digital position input. The components represent torque and flux in induction motors and active & reactive components in 3-phase power systems. Principally used for variable speed control, it is also useful in power-quality applications, such as harmonic and power-factor measurement, and frequency analysis.

The AD2S105's approach to extracting magnitude information simplifies filtering and A/D conversion. It operates on ±5-V supplies, accepts dc to 50-kHz input voltages, is housed in a 44-lead PLCC and operates from –40 to +85°C. Price is $6.99 in 1000s. **Circle 27**

Sinusoidal Oscillator

AD2S99 provides excitation, For resolvers and ac sensors

The AD2S99 is a low-cost programmable oscillator IC, available in a 20-pin PLCC package with an operating temperature range of –40 to +85°C. It is designed to provide excitation for resolvers and a wide variety of ac transducers. It also provides a synthesized reference signal, phase-locked to the Sin and Cos signals from the secondary windings of a resolver. This synchronizable reference signal dynamically compensates for temperature- and cabling-related phase shifts in a resolver-to-digital conversion system. A loss-of-signal (LOS) output indicates transducer failures.

Requiring no components, excitation frequencies of 2, 5, 10 or 20 kHz are pin-programmable. Other frequencies in this range are available with a pull-up resistor. Maximum frequency and amplitude errors are ±10% for the A grade. Price (100s) for the AD2S99AP is $6.98. **Circle 28**

Multiplexer Family

Combines fault protection And high performance

The ADG508F/509F/528F multiplexers are upgrades to industry-standard devices of similar type numbers (e.g., ADG508A/509A/528A). They combine fast switching (200-ns t_{ON} & t_{OFF}), low R_{ON} (300 Ω), and low leakage (±2 µA max, supplies *on* or *off*) with fault- and overvoltage protection. The **ADG508F & -528F** are 8-channel devices (ADG528F includes on-chip address and control latches), and the **ADG509F**, for differential applications, has 2 groups of 4 channels.

These latchup-proof devices can withstand continuous inputs up to ±35 V. When a fault occurs due to power supplies being turned off, all channels are turned off, with only a few nA of leakage current. With input overvoltage, the on channel is turned off, protecting circuits connected to the multiplexer. Break-before-make switching avoids channel-to-channel shorts. Prices (100s) start at $3.95. **Circle 26**

Low Dropout Voltage References

REF192/193/194/196 for 2.5, 3.0, 4.5, 3.3 volts Initial error < ±2 mV max; tempco < 5 ppm/°C max

The REF192/193/194/196 are the newest members of the REF19x family of precision bandgap references, joining the micropower, low-dropout (and up to 18-V single supply) 5-volt REF195 (*Analog Dialogue* 27-2, p. 27). They provide a variety of options for the designer of portable, micropower, and loop-current-powered instrumentation, A/D and D/A converters, & smart sensors.

The choices are summarized in the table. Maximum output current is 30 mA. All options are available in SO-8 packages; G grades are also available in plastic DIPs. In addition to the –40 to +85°C range, the devices are also specified for –40 to +125°C. Maximum quiescent current is 45 µA (15 µA in sleep mode). SO-8 prices in 1000s for E/F/G are $6.33/$3.04/$1.91. **Circle 29**

DEVICE COMPARISON (specs are max, –40 to +85°C)

	REF192	REF193	REF194	REF195	REF196
Nominal V_o, volts	2.5	3.0	4.5	5.0	3.3
Grades available	E, F, G	G	E, F, G	E, F, G	G
Tolerance, ±mV, 25°C	2, 5, 10	10	2, 5, 10	2, 5, 10	10
Tempco, ppm/°C	5, 10, 25	25	5, 10, 25	5, 10, 25	25
Line regulation, ppm/V	10, 20, 20	20	10, 20, 20	10, 20, 20	20
Load regulation, ppm/mA	15, 20, 20	20	10, 20, 20	10, 20, 20	20
Dropout V@ 10 mA (V)	1.00	0.8	0.5	0.5	0.8

Digital Audio: ASRC, Personal Sound, Codec

Stereo 16-Bit ASRC

AD1893 Asynchronous Sample-Rate Converter

The low-cost AD1893 SamplePort® Asynchronous Sample-Rate Converter is based on the AD1890 design (see *Analog Dialogue* 28-1, pp. 9-11). A digital-to-digital converter, it solves sample-rate and digital interconnect problems in audio applications for computer/communication and consumer equipment. It converts a fixed or changing input sample stream at an arbitrary sample rate to an output sample stream at a fixed or changing desired output sample rate, synchronizes streams that should be at the same sample rate, and rejects sample-rate clock jitter.

It runs on a +2.7 to +5.5-V supply. With 3.0 V, it dissipates 60 mW max (3 mW power-down). With a 16-MHz crystal, it samples word rates from 8 to 56 kHz with 96-dB dynamic range. It operates from –40 to +85°C, is housed in a 28-pin plastic DIP and 44-pin TQFP. Price (1000s) is $10.10 for either. **Circle 30**

Development Kit

Windows-based Personal Sound Architecture

The ADSC-SDK1 software development kit for sound-card products is based on the Personal Sound Architecture™ (more than 1/4 million already in use). PSA, a low-cost chipset (*Analog Dialogue* 27-2, p. 23), includes a 21xx-family DSP, AD184x codec, and an interface ASIC. The Kit provides software mechanisms for Windows applications and audio algorithms for 21xx DSPs to communicate within the Signal Computing Open-Programming Environment (SCOPE™). Third-party developers, integrators, and OEMs use it to develop Windows-based software for PSA-compatible platforms.

The SCOPE software includes DSP Manager, DSP Shell, SCOPE debugger, and an example of an audio application program written with a PC. It is bundled with the ADSP-21xx Family Software Development Tools package. Price is $395. **Circle 32**

Parallel-Port Codec

AD1846 for computer audio: Low cost, 1848-compatible

The AD1846 Soundport® 16-bit parallel-port stereo codec is a highly integrated "system on a chip" for computer-audio applications. It adds audio capabilities to computer mother boards and add-in cards. It supports Microsoft Windows™ Sound System-compatible applications, multimedia applications, and game audio interface devices. Pin- and register-compatible with the industry-standard AD1848, it operates from a single +5-V supply and can provide immediate cost savings in existing systems.

The AD1846 integrates key audio data-conversion and control functions into a monolithic IC requiring a minimal number of low-cost external support components. It provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses—and generates enable and direction controls for IC buffers such as the 74-245. The AD1846 supports one or two DMA channels for data transfer with the host computer, as well as programmed I/O.

Included on chip are stereo pairs of Σ–Δ A/D converters and D/A converters with low-pass anti-imaging output filters. The chip also contains digital decimation and interpolation filters. Selectable inputs to the ADCs (with independent software-controlled gains) include line, mic, aux, and post-mixed DAC output. ADC output data and DAC input data can be digitally mixed. DAC dynamic range exceeds 80 dB over the 20-kHz audio band, ADC dynamic range exceeds 70 dB, and sample rates from 5.5 kHz to 48 kHz are supported using external crystals. The pair of 16-bit ADC outputs is available over a byte-wide bidirectional interface that also supports 16-bit digital inputs to the DACs and control information. The AD1846 can accept and generate 16-bit twos-complement and 8-bit unsigned-magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

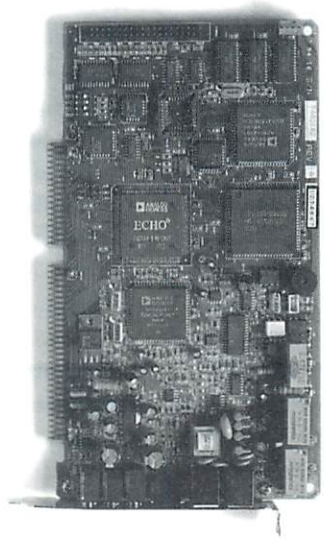
The device is housed in a 68-lead PLCC package. and operates at temperatures from 0 to +70°C. It is priced at $5.50 in 1000s. **Circle 33**

Design Guide & Chipset for PSCS IIa

ADDG-815 design guide and AD20msp815 chipset Facilitate design and construction of multipurpose card

The AD20msp815 chipset includes an ADSP-2101 digital signal processor, an AD1848 SoundPort®, an AD28msp01 modem signal port, an ESC614-1 audio ASIC (Echo Personal Sound System), and a DSI517X modem ASIC (Digicom SoftModem). Together they form the signal computing engine at the heart of Personal SoundComm™ System IIa, a reference design for an ISA-bus card that supports high-fidelity stereo audio, high-speed modem functions, and telephone answering machine functions.

The ADDG-815 is a Design Guide for PSCS IIa; it includes schematics, bill of materials, a PSCS IIa board, an eclectic set of software—including algorithm software licenses—and installation instructions for hardware and software. The chipset price is $62.20 (10,000s), and the design guide is $1500. **Circle 31**



Worth Reading

1994 FREE DESIGN-IN REFERENCE MANUAL

The 2400-page **1994 Design-In Reference Manual** includes data sheets on products most likely to be used by designers—New products, Outstanding best price-performance choices for new designs, and Highly popular products of long standing. The book combines and updates (and in some cases, abbreviates) the contents of our 1992 Converter, Amplifier, Audio/Video, and Special Linear Reference Manuals (a-k-a Databooks). **Free, Circle 34**

NEW BOOKS

Linear Design Seminar notes. This first complete revision since 1987 offers the basics of practical analog design, tailored to the entry-level design engineer or advanced college student—but useful to experienced designers as well. It includes discussions of amplifiers, comparators, analog multipliers & mixers, RMS-to-DC converters, sampled-data systems, data acquisition and conversion, voltage references, switches and muxes, sample-holds, transducer interfacing, filtering, practical hardware design techniques. 710 pages. 8 1/2" × 11" softcover, $25. Use book order card.

DSP Applications Using the ADSP-2100 Family, Volume 2. A companion to Volume 1, this volume's contents include more applications for 16-bit fixed-point DSPs: Modems; Linear predictive coding; GSM codec; Sub-band ADPCM; Speech recognition; Discrete cosine transform; Digital tone detection; Digital control system design; Variations on IIR biquad filters; Software UART; and Hardware interfacing. Published by Prentice Hall, it has 658 pages bound in softcover; a 3 1/2" high-density diskette is included. $30. Use book order card.

FREE BROCHURES AND GUIDES

New Products for Mil/Aero Applications. 16-pages of descriptions and block diagrams of ADCs, DACs, DSPs, MUXes and switches, amplifiers, references, plus a list of space-qualified products and information about MCM and hybrid capabilities. **Circle 35**

Digital Signal Processing. 24-page guide to Analog Devices products and capabilities in Digital Signal Processing: ADI's DSP philosophy, ADSP-21xx fixed-point and ADSP-21xxx floating-point (including SHARC—Super Harvard ARchitecture Computer) families, mixed-signal processors, development tools, hardware tools, digital audio, signal computing, support. **Circle 36**

DSP Quick Reference. The November, '94 edition of the 36-page *DSP Quick-Reference Manual* is available. A compact guide to selecting digital signal processors and development tools, it now incorporates summaries of the features, benefits, and applications of the ADSP-2181 and SHARC processors. **Circle 37**

Analog.Digital.Solutions. "Who is Analog Devices, and why should it matter?" Profusely illustrated Analog Devices corporate capabilities brochure discusses: our vision of signal processing's role in the future of electronics; computer products and DSP; communications products and wireless; transportation & industrial products and surface micromachining; standard-function products; capabilities and resources; customer support; global manufacturing and sales support; summary. **Circle 38**

A Tutorial in AC Induction and Permanent-Magnet Synchronous Motors—*Vector control with digital signal processors.* For anyone interested in motor control. Discusses the theory surrounding the control of permanent-magnet synchronous motors and ac induction motors, from slip and V-F drives to field-oriented flux-vector control. Covers the use of DSP in implementing the control algorithms and associated equations. Describes a family of coprocessors for motor control. 80 pages, softcover. **Circle 39**

SPICE Model Library. A 3 1/2" IBM PC-compatible diskette, Release J, July 94, has well over 400 macromodels, including 36 new models. Three voltage references are newly added—REF195, AD588, and AD680, along with the AMP04 single-supply instrumentation amplifier. **Circle 40**

SERIALS

DSPatch—The DSP Applications Newsletter: Number 31 (16 pages) features Trigem Sonamu-3 multimedia PC, which includes a multimedia board offering a variety of sound and telephony functions, including CD-quality record and playback, fax/modem, speakerphone, and answering machine capabilities. (Yes, it uses the ADSP-2101 processor, AD1848 SoundPort®, and AD28msp01 PSTN codec.). Also featured are Analogical Systems's Low-delay CELP (Code-Excited Linear Prediction) subsystem, based on the ADSP-2171, and a discussion of software for advanced digital telephony from Vocal Technologies, Ltd. Plus plugs for new products and conference exhibits; an impressive list of papers presented at ICSPAT'94 involving Analog Devices DSP applications; and regular features: Q & A, another installment of C Programming for DSP, workshops and application seminars, new software releases, book reviews, and available literature. **Circle 41**

APPLICATION NOTE

Make wide temperature-range, ultralow-drift accelerometers using low-cost crystal oven, by Charles Kitchin (AN-385—4 pp.). **Circle 42**

REPRINT

"GSM digital systems and implementation," by Rupert Baines, *Wireless Design & Development*, February, 1994, **Circle 46**

ADI AUTHORS IN THE TRADE PRESS

[Reprints not available from Analog Devices]

In *Electronic Design*'s special analog issue, 7 Nov., 1994:

"Design video circuits using high-speed op amp systems," by Walt Jung and Scott Wurcer. (10 pages

"Drive circuitry is critical to high-speed sampling ADCs," by Walt Kester. (8 pages)

"Tailor microphone preamps to get optimum results," by Walt Jung and Adolfo Garcia. (2 pages)

"Oscillator keeps THD below 1 ppm," by Jeff Smith. Design idea in *EDN*, 10 Nov., 1994.

"Maximize dynamic range in CCD-based imaging systems," by Steve Ruscak. *EDN*, 27 Oct., 1994. 6 pages showing circuits and tradeoffs.

"Function generator is stable, accurate," by Moshe Gerstenhaber and Mark Murphy. Idea for design in *Electronic Design*, 25 October, 1994

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

CHANGES & ERRATA • • • **Analog Dialogue 28-2**, p. 30, the *ADSP-2100 Family User's Manual* has 448 pages (not 458) • • • **AD7010 and AD7011** data sheets, **Rev. B is now available**. Includes changes in Fig. 1, signal vector magnitude spec, and some timing specs. **Circle 44** • • • **AD7013** data sheet, **Rev. A is now available**. Includes a change in power-down spec to 10 µA. **Circle 45** • • • **A redesign that improved the AD7512DI**'s performance, including switching time, also increased susceptibility of the logic inputs to oscillations on the V_{SS} line if the supplies are not decoupled. Minimize such problems with high-performance analog ICs by routinely decoupling them with 0.1-µF capacitors across the supply terminals.

PCMCIA • • • **More than 150 Analog Devices product types, in just about every category,** are available with **maximum package thickness ≤1.78 mm** for applications within the 2.00 mm thickness constraint of PCMCIA (Personal Computer Memory Card International Association) cards. **Included are** ADCs and DACs, switches, references, multiplexers, op amps log amps, audio & video amps, mixers, sample-holds, temperature sensors, codecs, sample-rate converters, DSPs, RS-232 and -485 transceivers, and supervisory circuits. Call our sales force (page 24) for information.

IN THE LAST ISSUE

Volume 28, Number 2, 1994, 32 Pages
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DSP NEWS • • • The **ADSP-2171** (*Analog Dialogue* 28-1, p. 22) is now available in **33-MIPS versions, and at reduced prices**. Also available is the **ADSP-2173**, with dissipations as low as **70 mW, for power-sensitive 3.3-volt applications** in battery-operated and portable equipment • • • The **AD20msp815** chip set (see page 21) is being used in (major Korean manufacturer) **Trigem's Sonamu-3 personal computer**, to provide a variety of sound and telephony functions, including CD-quality record and playback, fax/modem, speakerphone and answering-machine capabilities • • • The **ADSP-2166** (a member of the ADSP-216x family introduced in *Analog Dialogue* 28-1, p. 22), a **3-volt ROM-coded processor**, was chosen by **Inmarsat for the heart of their Global Satellite Paging System**. The DSP in the pager decodes the information received from the satellite, filtering out noise and interference. Substituting for antenna gain, sophisticated techniques permit detection of weak signals with smaller, more-portable devices. Five companies in the U.S., Germany, Japan, and Denmark are manufacturing the completed pagers.

MILITARY • • • The **AD600, AD602, and AD603** are exponential-gain-control X-Amp™ amplifiers, providing wideband performance and precise **gains in dB/volt of control voltage**. They are now available qualified to MIL-STD 883 • • • The **AD676 16-bit, 100-ksps A/D converter** is now available in a /883 version and specified by standard military drawing **(SMD) 5962-94743**.

SHOWS • • • Current plans call for Analog Devices to be in these (and other) shows during 1995. If you're in the neighborhood, come see us • • • **Wireless Symposium**, Santa Clara, CA, 15-17 February • • • **WinHEC** '95, San Francisco CA, 20-22 March • • • **DSPx '95**, San Jose CA, 16-18 May • • • **Computex Taipei '95**, Taipei, Taiwan, 5-9 June • • • **Sensors Expo '95**, Rosemont IL, 12-14 September • • • **Telecom '95**, Geneva, Switzerland, 3-11 October • • • **Comdex/F 95**, Las Vegas NV, 13-17 November.

PATENTS • • • 5,313,165 to A. Paul Brokaw for **Temperature-compensated apparatus for monitoring current having controlled sensitivity to supply voltage** • • • 5,321,404 to A. Martin Mallinson, Peter R. Holloway, Geoffrey P. O'Donoghue, and Charles H. Ayres for **Ripsaw analog-to-digital converter and method** • • • 5,323,121 to James R. Butler for **Folded cascode operational amplifier with gain-enhancing base-current compensation** • • • 5,323,122 to Derek F. Bowers for **Rapid slewing unity-gain buffer amplifier with boosted parasitic capacitance charging** • • • 5,323,158 to Paul F. Ferguson, Jr., for **Switched-capacitor one-bit digital-to-analog converter** • • • 5,326,726 to Robert W. K. Tsang and Theresa A. Core for **Method for fabricating monolithic chip containing integrated circuitry and suspended microstructure** • • • 5,327,030 to Lawrence M. DeVito and A. Paul Brokaw for **Decoder and monolithic integrated circuit incorporating same** • • • 5,331,221 to Apparajan Ganesan, Paul F. Ferguson, Jr., and David H. Robertson for **Gain linearity correction for MOS circuits** • • • 5,339,018 to A. Paul Brokaw for **Integrated circuit monitor for storage battery voltage and temperature** • • • 5,339,021 to David Thomson for **Cascaded resistance ladder attenuator network** • • • 5,341,033 to Gregory T. Koker for **Input buffer circuit with deglitch method and apparatus** • • • 5,341,403 to Sean Morley for **Means to avoid data distortion in clock-synchronized signal sampling** • • • 5,343,196 to Stephen W. Harston for **D/A converter with reduced power consumption** • • • 5,345,185 to Barrie Gilbert for **Logarithmic amplifier gain stage** • • • 5,345,824 to Steven J. Sherman, A. Paul Brokaw, Robert W. K. Tsang, and Theresa Core for **Monolithic accelerometer** • • • 5,347,224 to A. Paul Brokaw for **Current-monitoring circuit having controlled sensitivity to temperature and supply voltage** • • • 5,352,973 to Jonathan M. Audy for **Temperature compensation bandgap voltage reference and method** • • • 5,353,026 to James Wilson for **FIR filter with quantized coefficients and coefficient quantization method** • • • 5,363,102 to Paul F. Ferguson, Jr., for **Offset insensitive switched-capacitor gain stage**.

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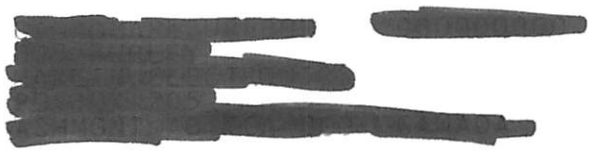

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